64Mb Quad SPI MRAM

Single/Dual/Quad SPI MRAM

3.3V/1.8V

- **S3A6404V6M**
- **S3A6404R6M**

Datasheet

Feature

- 64Mb: Dual Stack of two 32Mb
- Serial Peripheral Interface with Mode 0 and Mode 3
  - two CS# (CS1#, CS2#) configuration
  - Single and double data rate (SDR/DDR)
- Performance
  - 108MHz for SDR
  - 54MHz for DDR
- Supports XIP for read and write operations
- Data protection
  - WP# pin write protection
  - Block lock protection
- Nonvolatile status and configuration registers
- Identification
  - Unique ID
  - Serial number - user writable
- Augmented nonvolatile-area
- Memory cell: STT-MRAM
- Density
  - 64Mb
- Data Integrity: No external ECC required
- Data Endurance
  - Unlimited read cycle
  - 10^{14} write cycles
- Data Retention
  - 10 years at 85°C
- Single Power Supply Operation
  - S3A6404V6M: 2.70V~3.60V
  - S3A6404R6M: 1.71V~1.98V
- Operating Temperature Range
  - Industrial Temperature: -40°C to 85°C
- RoHS compliant package
  - 24-BGA (6.0mm x 8.0mm)

Performance

Operation	Typical Values		Units
	1.8V(S3A6404R6M)	3.3V(S3A6404V6M)	
Frequency(SDR)	108 (Max.)		MHz
Frequency(DDR)	54 (Max.)		MHz
Standby Current	1.2	1.4	mA
Deep Power Down Current	120	340	µA
Active Read Current (4-4-4) SDR @108MHz	10	15	mA
Active Write Current (4-4-4) SDR @108MHz	26	32	mA

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1. General Description

The device is a Spin-Transfer-Torque Magneto-resistive Random Access Memory (STT-MRAM).
It features a SPI bus interface, XIP (execute-in-place) functionality and hardware and software based data protection mechanisms.
SPI (Serial Peripheral Interface) is a synchronous serial communication interface with command, address, and data signals.

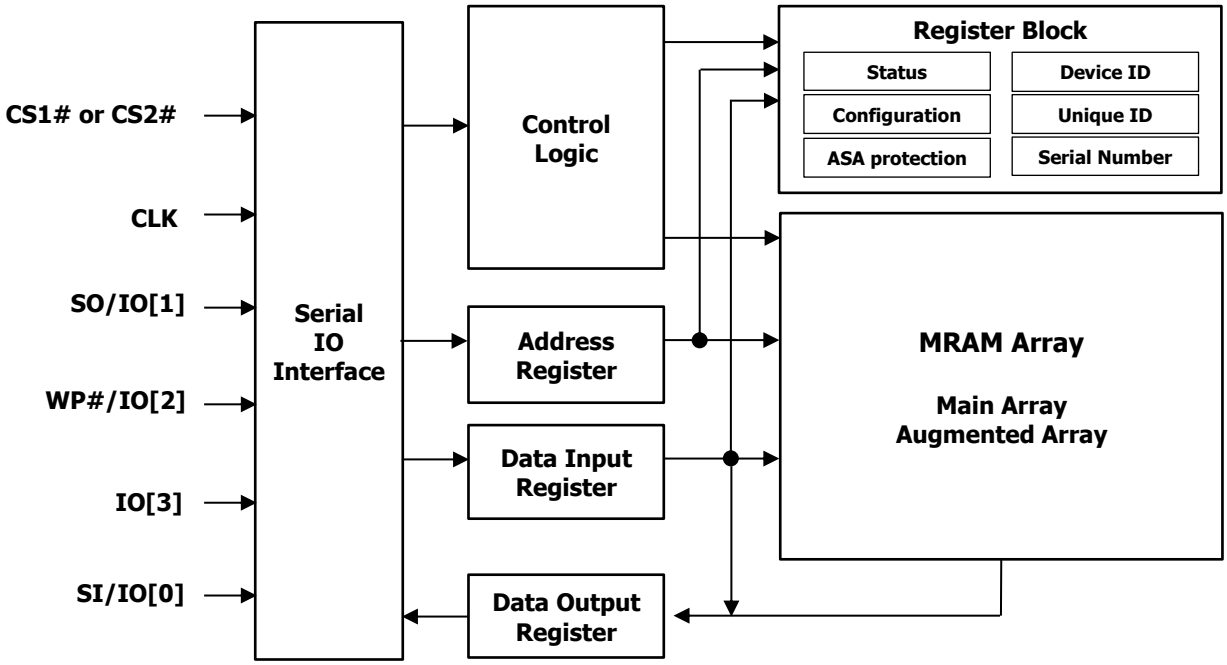
The device consists of two 32Mb quad SPI devices, providing 4-bit I/O data access with a 2-CS#/1-CLK configuration. Each individual die can be active by its own chip select signal.

Each individual die provides various SPI modes, allowing options for bandwidth expansion. Extended SPI mode has a single pin for the command signal for each die. The user can select an option for how many pins to be allocated for address, and data signals among 1 pin, 2 pins or 4 pins. Dual SPI mode provides 2 pins for command, address and data signals. Quad SPI mode provides 4 pins for command, address and data signals.

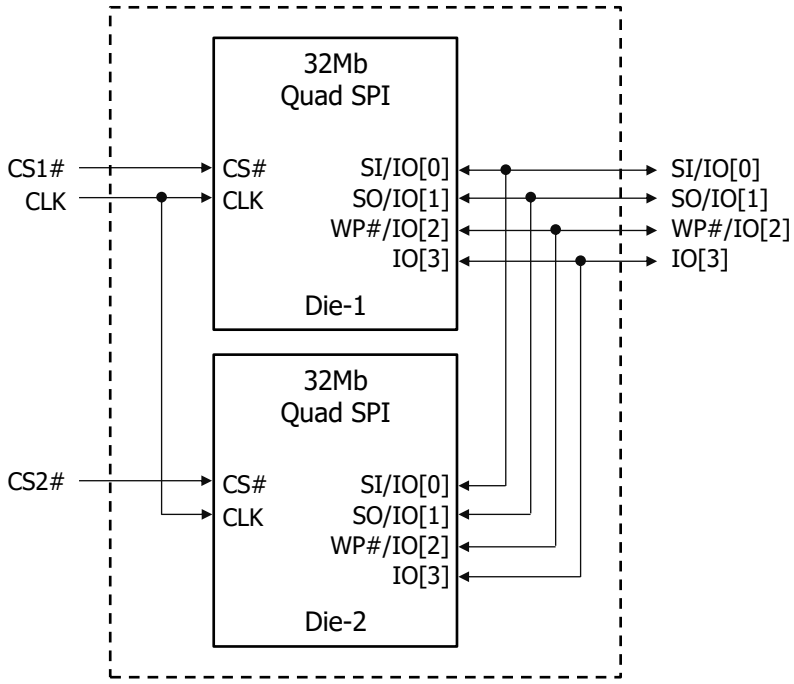
Each individual die has its own nonvolatile register bits – status register, configuration register, serial number register, augmented 512-byte register, protection register for augmented bytes, device ID, and unique ID. The status register and configuration register are required to be set at least once on power-up after the high temperature solder-reflow process for each individual die.

The device is available in small footprint 24-BGA package. The package is compatible with similar non-volatile products. The device is offered with an industrial (-40°C to 85°C) operating temperature range.

Figure 1: Functional Block Diagram



Functional Block Diagram for each individual die


32Mb
Quad SPI
CS1#
CLK
CS#
CLK
SI/IO[0]
SO/IO[1]
WP#/IO[2]
IO[3]
Die-1
SI/IO[0]
SO/IO[1]
WP#/IO[2]
IO[3]
32Mb
Quad SPI
CS2#
CS#
CLK
SI/IO[0]
SO/IO[1]
WP#/IO[2]
IO[3]
Die-2

2. Pin Configuration

Figure 2: 24-Ball BGA, 5x5 (Balls Down)

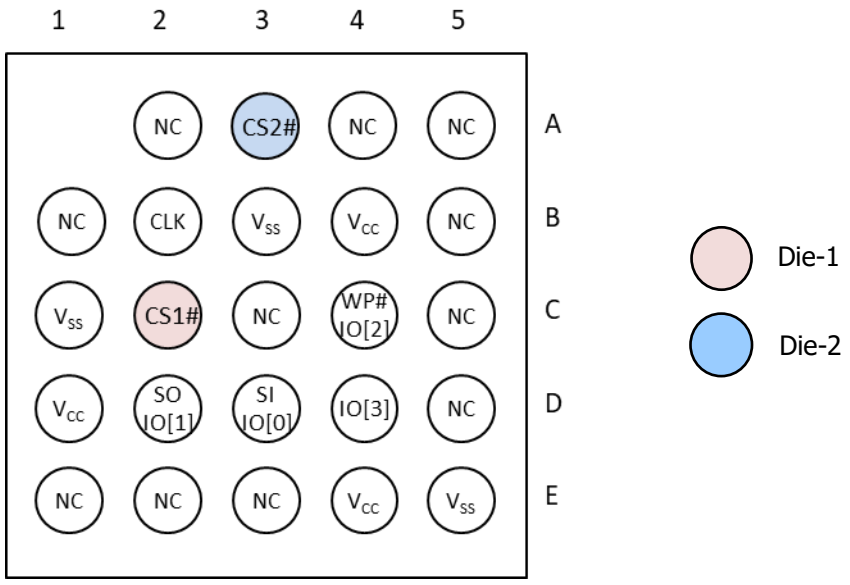


Table 1: Pin Description

Pin	Type	Description
CS1#, CS2#	Input	**Chip Select:** When CS1# or CS2# is driven Low, a read or write operation is initiated. When CS1# and CS2# are driven High, the device enters standby mode, and all other input pins are ignored and the output pins are tri-stated. CS1# and CS2# should be High at power-up to prevent abnormal write operation. These pins do not have internal pull-up resistor.
CLK	Input	**Clock**: In SDR (single data rate) mode, the command, address, and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. In DDR (double data rate) mode, the command is latched on the rising edge of the clock and address and data inputs are latched on the rising and falling edges of the clock. Similarly, data is output on both edges of the clock. The two SPI clock modes are supported as follows. • SPI Mode 0 : SDR and DDR • SPI Mode 3 : SDR only
WP#/IO[2]	Input /Bidirectional	**Write Protect (Extended SPI):** The writing of status and configuration registers is protected in related with WP# and WPEN. See "Table 8: Write Protection Modes". This pin does not have an internal pull-up resistor, it cannot be left floating and must be driven. WP# is valid in Extended SPI and Dual SPI. **IO[2] :** The bidirectional I/O in Quad input/output mode.
IO[3]	Bidirectional	**IO[3] :** The bidirectional I/O in Quad input/output modes.
SI/IO[0]	Input /Bidirectional	**SI:** The serial input in Single input mode. **IO[0]:** The bidirectional I/O in Dual and Quad input/output modes
SO/IO[1]	Output /Bidirectional	**SO:** The serial data output in Single output mode. **IO[1] :** The bidirectional in Dual and Quad input/output modes.
Vcc	Supply	Power pin
Vss	Supply	Ground pin

3. Power On/Off Sequence

3.1 Power On/Off Sequence for 3.3V Device

During power-up, power-down, or power-loss, both CS1# and CS2# must follow Vcc to ensure data protection.
It is recommended that both CS1# and CS2# must follow Vcc when Vcc is below Vcc(minimum) and during t_{PU}.
A 10KΩ pull-up resistor between Vcc and both CS1# and CS2# pins is recommended.
Normal operation must start after t_{PU}.

Figure 3: Power-up/down Behavior for 3.3V Device

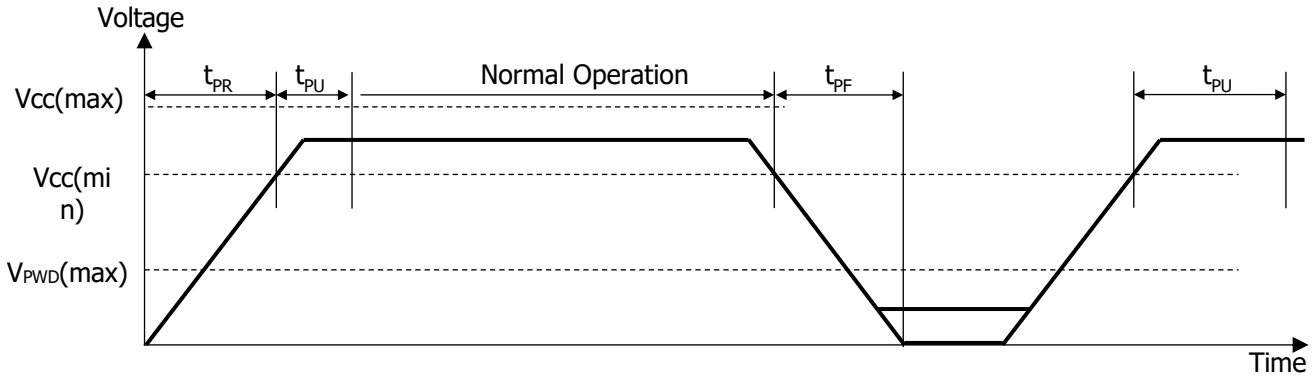


Table 2: Power Up/Down Timing for 3.3V Device

Parameter	Symbol	Min	Max	Units
Vcc Range	Vcc	2.7	3.6	V
Vcc rising time	t_{PR}(1)	30	-	µs/V
Vcc falling time	t_{PF}(1)	30	-	µs/V
Vcc(min) to CS# Low (first instruction) time	t_{PU}(1)	2.0	-	ms
Vcc needed to below V_{PWD} for ensuring initialization will occur	V_{PWD}(1)	-	1.6	V

Notes:
1: These parameters are guaranteed by characterization; not tested in production.
2: CS# denotes CS1# or CS2#.

3.2 Power On/Off Sequence for 1.8V Device

During power-up, power-down or power-loss, both CS1# and CS2# must follow Vcc to ensure data protection.
It is recommended that both CS1# and CS2# must follow Vcc when Vcc is below Vcc(minimum) and during t_{PU}.
A 10KΩ pull-up resistor between Vcc and both CS1# and CS2# pins is recommended.
Software reset operation is required after t_{PU} for both dies.
Normal operation must start after t_{SRST}.

Figure 4: Power-up/down Behavior for 1.8V Device

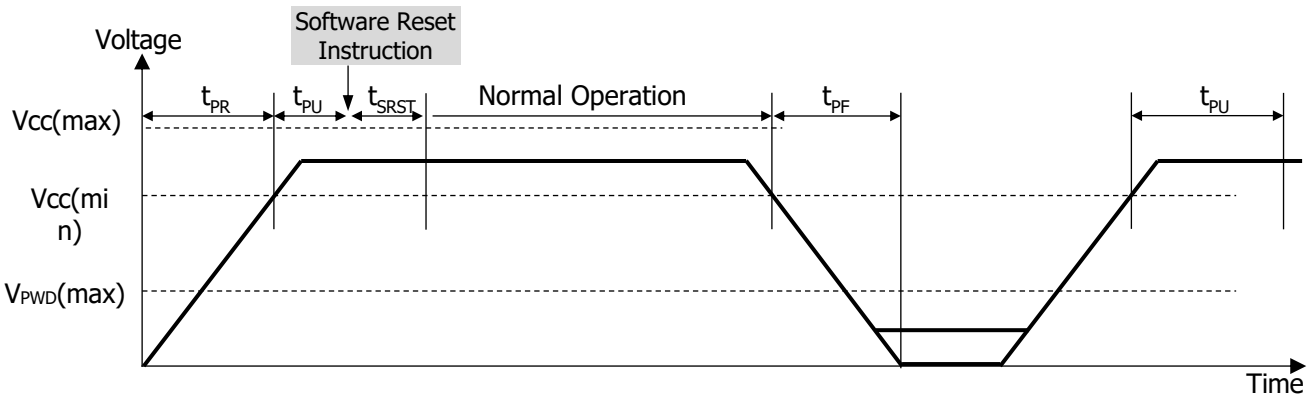


Table 3: Power Up/Down Timing for 1.8V Device

Parameter	Symbol	Min	Max	Units
Vcc Range	Vcc	1.71	1.98	V
Vcc rising time	t_{PR}(1)	30	-	µs/V
Vcc falling time	t_{PF}(1)	30	-	µs/V
Vcc(min) to CS# Low (first instruction) time	t_{PU}(1)	2.0	-	ms
Vcc needed to below V_{PWD} for ensuring initialization will occur	V_{PWD}(1)	-	0.8	V
Software Reset time	V_{SRST}(1)	2.0		ms

Notes:
1. These parameters are guaranteed by characterization; not tested in production.

4. Memory Organization

Table 4: Memory Map

Density	Address Range	24-bit Address [23:0]	
32Mb -each individual die	000000h – 3FFFFFh	[23:22] – Logic '0'	[21:0] – Addressable

Table 5: Augmented Area Map

Augmented Area	Address Range	24-bit Address [23:0]	
512-byte -each individual die	000000h – 0001FFh	[23:9] – Logic '0'	[8:0] – Addressable

Notes:
1. The augmented 512-byte area is divided into 8 individually readable and writable sections (64 bytes per section). After an individual section is written, it can be protected individually to prevent further writing. The address bits Address[23:9] must be logic '0'.

Table 6: Register Address Map

The device provides register read/write instructions to read and write data of each register.
In addition, the device provides the register read and/or write function based on addresses using RDAR(65h) and WRAR(71h) commands.

Register Name	Address for each individual die
Status Register	0x000000h
Configuration Register 1	0x000002h
Configuration Register 2	0x000003h
Configuration Register 3	0x000004h
Configuration Register 4	0x000005h
Device Identification Register	0x000030h
Unique Identification Register	0x000040h
Serial Number Register	0x000080h

Notes:
1. Register address space is different from the memory array and augmented 512-byte area.

5. Register Description

Each individual die has its own nonvolatile registers – Status Register, Configuration Register, Serial Number Register, Augmented Area Register, Protection Register for augmented area, Device ID, and Unique ID. The nonvolatile bits of Status Register and Configuration Register are required to be set at least once on power-up after high temperature solder-reflow process for both dies. The device configuration is set from Status Register and Configuration Registers after power-up or by Write Register instructions. The following descriptions apply to each individual die.

5.1 Status Register

The device offers both hardware and software based data protection schemes. Hardware protection is through WP# pin. Software protection is controlled by configuration bits in the Status register. Both schemes inhibit writing to the registers, memory and augmented area. Status Register contains options for enabling/disabling data protection.
By controlling configuration bits in Status Register, user can protect data in memory based on software protection schemes. The Status Register can be written using either the Write Status Register instruction or Write Any Register (Address based) instruction combined with CR1[2] of Configuration Register 1, and it can be read using either Read Status Register instruction or Read Any Register(Address based) instruction.

Table 7: Status Register

Bits	Name	Read/ Write	Default State	Description
SR[7]	WPEN	R/W	-	Hardware Based WP# Protect Bit 1: Protection Enabled – write protects when WP# is Low 0: Protection Disabled – Doesn't write protect when WP# is Low
SR[6]	SNPEN	R/W	-	Serial Number Protect Bit 1: Serial Number Write protected 0: Serial Number Writable
SR[5]	TB	R/W	-	Top/Bottom Memory Array Protect Selection 1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range)
SR[4]	BP[2]	R/W	-	Block Protection Bits
SR[3]	BP[1]	R/W	-	
SR[2]	BP[0]	R/W	-	
SR[1]	WREN	R	0	Write Protection Enable 1: Write Operation Protection Disabled 0: Write Operation Protection Enabled
SR[0]	RSVD	R	-	Reserved for future use

Notes:
1. SR[7:2] are nonvolatile bits.
2. TB and BP[2:0] can be protected by CR1[2] of Configuration Register 1.

5.1.1 Write Protection Modes

WPEN bit (SR[7]) is used in conjunction with the WREN bit (SR[1]) and the WP# pin to provide hardware block protection. SR[7:2] will remain set from the nonvolatile registers whenever the power is on. The WREN bit is volatile and set to '1' by the Write Enable command. It is reset to '0' after power up, software reset, JEDEC reset, Write Disable command, or when Write Register operation finishes. For WREN information on write operations for memory and augmented area, please refer to Configuration Register 4.
The device enters hardware protection when the WP# input is Low and the WPEN bit of Status Register is set to '1', and the nonvolatile registers cannot be changed. The device exits from hardware protection when the WP# pin goes High or WPEN bit is set to '0', and the register bits can be changed.

Table 8: Write Protection Modes

WREN	WPEN	WP#	Registers(1)	Memory(2) and Augmented 512-byte Area(3)	
				Protected Area	Unprotected Area
0	X	X	Protected	Protected	Protected
1	0	X	Unprotected	Protected	Unprotected
1	1	0	Protected	Protected	Unprotected
1	1	1	Unprotected	Protected	Unprotected

Notes:
1. Status, Configuration, Protection for Augmented 512-Byte Area and Serial Number Register.
2. Memory address range protection based on Block Protection Bits
3. The Augmented 512-byte Area range protection based on Augmented 512-Byte Area Protection Register. The Augmented 512-byte Area can also be protected by CR1[0] of Configuration Register 1.
4. The Serial Number register can also be protected by SR[6] of Status Register.
5. X: Don't Care – can be logic '0' or '1'
6. Protected: write protected, Unprotected: writable

5.1.2 Block Protection

The write protection blocks for the memory array are determined by the status register bits (TB and BP[2:0]) as Table 8 below. TB and BP[2:0] can be modified by Write Status Register instruction(01h) or Write Any Register instruction(71h) when the WP# is High or the Status Register WPEN bit is set to '0' and CR1[2] of Configuration Register 1 is set to '0'.

Table 9: Block Protection Address Range Selection

TB	BP[2]	BP[1]	BP[0]	Protected Portion	32Mb for each individual die
0/1	0	0	0	None	None
0	0	0	1	Upper 1/64	3F0000h – 3FFFFFh
0	0	1	0	Upper 1/32	3E0000h – 3FFFFFh
0	0	1	1	Upper 1/16	3C0000h – 3FFFFFh
0	1	0	0	Upper 1/8	380000h – 3FFFFFh
0	1	0	1	Upper 1/4	300000h – 3FFFFFh
0	1	1	0	Upper 1/2	200000h – 3FFFFFh
1	0	0	1	Lower 1/64	000000h – 00FFFFh
1	0	1	0	Lower 1/32	000000h – 01FFFFh
1	0	1	1	Lower 1/16	000000h – 03FFFFh
1	1	0	0	Lower 1/8	000000h – 07FFFFh
1	1	0	1	Lower 1/4	000000h – 0FFFFFh
1	1	1	0	Lower 1/2	000000h – 1FFFFFh
0/1	1	1	1	All	000000h – 3FFFFFh

5.1.3 Augmented Area Protection

The Augmented Area Protection register contains options for enabling/disabling data protection for eight sections.

Table 10: Augmented Area Protection Register – Read and Write

Bits	Name	Address Range for each individual die	Read/ Write	Default State	Description
ASP[7]	ASPS[7]	0001C0h – 0001FFh	R/W	0	1: Protection Enabled 0: Protection Disabled
ASP[6]	ASPS[6]	000180h – 0001BFh	R/W	0	
ASP[5]	ASPS[5]	000140h – 00017Fh	R/W	0	
ASP[4]	ASPS[4]	000100h – 00013Fh	R/W	0	
ASP[3]	ASPS[3]	0000C0h – 0000FFh	R/W	0	
ASP[2]	ASPS[2]	000080h – 0000BFh	R/W	0	
ASP[1]	ASPS[1]	000040h – 00007Fh	R/W	0	
ASP[0]	ASPS[0]	000000h – 00003Fh	R/W	0	

Notes:
1. ASP[7:0] are nonvolatile bits.
2. The Augmented 512-byte area can also be protected by CR1[0] of Configuration Register 1.

5.2 Configuration Register

The Configuration Register can be configured using either the Write Configuration Register instructions or Write Any Register(Address based) instruction, and it can be read using either Read Configuration Register instructions or Read Any Register(Address based) instruction.

5.2.1 Configuration Register 1

Configuration Register 1 controls the locking and unlocking of data protection options set in the Status Register and Augmented 512-Byte Area Protection Register. Once locked, these protection options cannot be changed in the Status register.

Table 11: Configuration Register 1

Bits	Name	Read/Write	Default State	Selection Options
CR1[7:3]	RSVD	R/W	-	Reserved for future use
CR1[2]	MAPLK	R/W	-	Status Register TB, BP[2:0] Protect 1: Lock TB and BP[2:0] 0: Unlock TB and BP[2:0]
CR1[1]	RSVD	R/W	-	Reserved for future use
CR1[0]	ASPLK	R/W	-	Augmented Area Data Protection 1: Write Protection for Augmented Area Data regardless of ASP[7:0] 0: Write Protection for Augmented Area Data depending on ASP[7:0]

Notes:
1. CR1[7:0] are nonvolatile bits.

5.2.2 Configuration Register 2

Configuration Register 2 controls the interface types along with memory array access latency.

Table 12: Configuration Register 2

Bits	Name	Read/Write	Default State	Description
CR2[7]	RSVD	R/W	-	Reserved for future use
CR2[6]	QPIEN	R	0	Quad SPI (QPI 4-4-4) Interface Mode 1: Quad SPI (QPI 4-4-4) Enabled 0: Quad SPI (QPI 4-4-4) Disabled
CR2[5]	RSVD	R/W	0	It must be written as '0'
CR2[4]	DPIEN	R	0	Dual SPI (DPI 2-2-2) Interface Mode 1: Dual SPI (DPI 2-2-2) Enabled 0: Dual SPI (DPI 2-2-2) Disabled
CR2[3]	RL[3]	R/W	-	Read Latency Selection Bits 0000: 0 Cycle 1000: 8 Cycles 0001: 1 Cycle 1001: 9 Cycles 0010: 2 Cycles 1010: 10 Cycles 0011: 3 Cycles 1011: 11 Cycles 0100: 4 Cycles 1100: 12 Cycles 0101: 5 Cycles 1101: 13 Cycles 0110: 6 Cycles 1110: 14 Cycles 0111: 7 Cycles 1111: 15 Cycles
CR2[2]	RL[2]		-	
CR2[1]	RL[1]		-	
CR2[0]	RL[0]		-	

Notes:
1. Read Latency is frequency-dependent.
2. Read(03h) does not depend on the Read latency Selection Bits CR2[3:0].
3. CR2[7,5,3:0] are non-volatile bits.
4. CR2[5] must be written as '0'.
5. Extended SPI is enabled when both CR2[6] and CR2[4] are '0'.

The number of read latency cycles must be set to accord with the clock frequency for all Read Memory instructions (except for Read 03h) and Read Augmented 512-Byte Area (4Bh). Insufficient read latency cycles for the operating frequency causes the device to read incorrect data.

Table 13: Read Latency Cycles vs. Maximum Frequency (Memory Area)

Read Latency Cycles	SDR			DDR			Unit
	1s-1s-1s	1s-1s-2s 1s-2s-2s 2s-2s-2s	1s-1s-4s 1s-4s-4s 4s-4s-4s	1s-1d-1d	1s-1d-2d 1s-2d-2d 2s-2d-2d	1s-1d-4d 1s-4d-4d 4s-4d-4d	
0	108	40	20	-	-	-	MHz
1	108	66	33	54	-	-	MHz
2	108	83	50	54	33	33	MHz
3	108	100	66	54	40	40	MHz
4	108	108	83	54	54	54	MHz
5	108	108	100	54	54	54	MHz
6~15	108	108	108	54	54	54	MHz

Notes:
1. Read(03h) does not depend on Read latency Selection Bits CR2[3:0]. The latency of Read(03h) is always 0-cycle.

Table 14: Read Latency Cycles vs. Maximum Frequency (Augmented Area)

Read Latency Cycles	RDAS 4Bh	Unit
	1s-1s-1s	
0~2	NA	-
3	33	MHz
4	54	MHz
5	66	MHz
6	83	MHz
7	100	MHz
8~15	108	MHz

Table 15: Read Latency Cycles vs. Maximum Frequency (Read Any Register)

Read Type	XIP	Latency Cycles	Max Frequency
1s-1s-1s (RDAR 65h)	-	8	108MHz
2s-2s-2s (RDAR 65h)	-	4	108MHz
4s-4s-4s (RDAR 65h)	-	2	108MHz

Notes:
1. RDAR(65h, read any register instruction) does not depend on Read latency Selection Bits CR2[3:0].

5.2.3 Configuration Register 3

Configuration Register 3 controls the output driver strength along with the boundary size of read data wrapping.

Table 16: Configuration Register 3

Bits	Name	Read/Write	Description
CR3[7]	DRV[2]	R/W	Output Driver Strength Selection DRV[2:0] 3.3V 1.8V 000: 36Ω 35Ω 001: 100Ω 95Ω 010: 75Ω 63Ω 011: 60Ω 50Ω 100: 48Ω 40Ω 101: 41Ω 30Ω 110: 29Ω 26Ω 111: 24Ω 22Ω
CR3[6]	DRV[1]		
CR3[5]	DRV[0]		
CR3[4]	WRPEN	R/W	Read WRAP Enable 1: Read Wrap Enabled 0: Read Wrap Disabled
CR3[3]	RSVD	R/W	Reserved for future use
CR3[2]	WRPL[2]	R/W	Wrap length configuration WRPL[2:0] 000: 16-byte wrap 001: 32-byte wrap 010: 64-byte wrap 011: 128-byte wrap 100: 256-byte wrap 101: 512-byte wrap 110: 1K-byte wrap 111: Reserved
CR3[1]	WRPL[1]		
CR3[0]	WRPL[0]		

Notes:
1. Default output strength is DRV[2:0]=000.
2. CR3[7:0] are non-volatile bits.

	Description
WRPEN(CR3[4]) =Low	Read and write operation: continuous mode Read or write operation starts at the input address, and once the address reaches the maximum address boundary for each individual die, it automatically returns to minimum address (000000h) until CS# goes to High.
WRPEN(CR3[4]) =High	Read operations: wrap mode Read wrap mode is enabled when WRPEN(CR3[4]) is High, and the read data wrap length is controlled by WRPL[2:0]. The output data starts at the input address, data are output sequentially. Once it reaches the ending boundary, the output will wrap around to the beginning boundary automatically until CS# is pulled High. Write operation: continuous mode Write operation starts at the input address, and once the address reaches the maximum address boundary, it automatically returns to minimum address (000000h) until CS# goes to High.

5.2.4 Configuration Register 4

Configuration Register 4 controls Write Protection Enable/Disable (WREN) functionality during memory and augmented area writes.
This functionality makes SPI MRAM compatible to other SPI devices.

Table 17: Configuration Register 4

Bits	Name	Read/Write	Default State	Selection Options
CR4[7:2]	RSVD	R/W	-	Reserved for future use
CR4[1]	WRENS[1]	R/W	-	00: Normal mode WREN is prerequisite for every Memory or Augmented Area Write instruction (WREN is reset after CS# goes High). 01: SRAM mode WREN is not a prerequisite for Memory Write or Augmented Area Write instructions (WREN is ignored). 10: Back-to-Back mode WREN is prerequisite only to the first Memory Write or Augmented Area Write instruction. To reset WREN, WREN Disable instruction must be executed. (WREN does not reset after CS# goes High). 11: Reserved
CR4[0]	WRENS[0]		-	

Notes:
1. Write Protection Enable (WREN – Status Register) for Register is maintained irrespective of the Configuration Register 4 settings.
   In other words, all register write Instructions require WREN to be set, and WREN is reset after CS# goes High.
   CR4[1:0] only affects writing for memory and augmented area.
2. CR4[7:0] are nonvolatile bits.

5.3 Device Identification Register

Each individual die has Device Identification register which contains Netsol's Manufacturing ID along with device configuration information.

Table 18: Device Identification Register

Bits	Manufacturer ID	Device Configuration				
ID[31:0]	ID[31:24]	Interface	Voltage	Temperature	Density	Reserved
		ID[23:20]	ID[19:16]	ID[15:12]	ID[11:8]	ID[7:0]

Manufacturer ID	Interface	Voltage	Temperature	Density	Reserved
31-24	23-20	19-16	15-12	11-8	7-0
1101 1001	0000 : Quad SPI	0001 : 3.3V 0010 : 1.8V	0000 : -40ºC~85ºC	0110 : 32Mb	00000001

5.4 Serial Number Register

Each individual die provides 64-bit Serial Number register and the user can write it.

Table 19: Serial Number Register

Bits	Name	Description	Read/ Write	State
SN[63:0]	SN	Serial Number Value	R/W	User writable

Notes:
1. Serial Number Bits are nonvolatile.
2. User should write the data after solder-reflow process, if used.

5.5 Unique Identification Register

Unique Identification register contains a number unique for each individual die.

Table 20: Unique ID Register

Bits	Name	Read/Write	Description
UID[63:0]	UID	R	Unique Identification Number Value The value stored is factory-written in the factory and specific to each device.

6. SPI Protocol

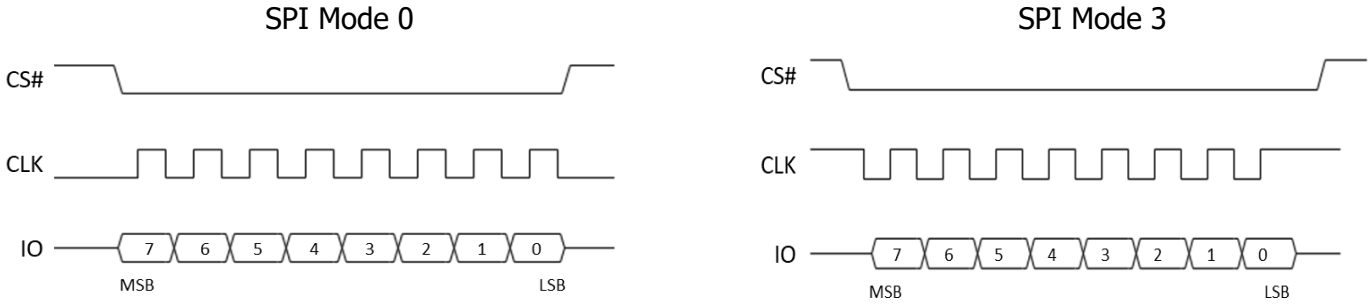
All communication between a host and the device occurs through commands. The commands define the operations that need to be executed. Instructions consist of a command followed by an optional address modifier and the associated data, which are transferred sequentially. To initiate a command, CS# should be driven Low and CLK should be toggled.
When the correct command is input to this device, it enters active mode and remains in that state until next CS# rising edge. When CS# goes High, the device goes into standby mode.

6.1 SPI Clock Modes

The following two SPI clock modes are supported.

- SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR
- SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only

Figure 5: SPI Clock Modes



Mode0: Clock stays in Low level during idle state and starts toggling by going High.

Mode 3: Clock stays in High level during idle state and starts toggling by going Low.

6.2 SPI Interface Modes

Each individual die supports 3 categories of SPI interface modes.

1. Extended SPI: the command is transferred through one pin.
   1) Address and data are transferred through one pin (1-1-1).
   2) Address is transferred through one pin, data is transferred through two pins (1-1-2).
   3) Address is transferred through one pin, data is transferred through four pins (1-1-4).
   4) Address and data are transferred through two pins (1-2-2).
   5) Address and data are transferred through four pins (1-4-4).
2. Dual SPI: All command, address and data are transferred through two pins (2-2-2).
3. Quad SPI: All command, address and data are transferred through four pins (4-4-4).

The device supports DDR (double data rate) for address and data.

Table 21: Pin Assignment / Interface Modes

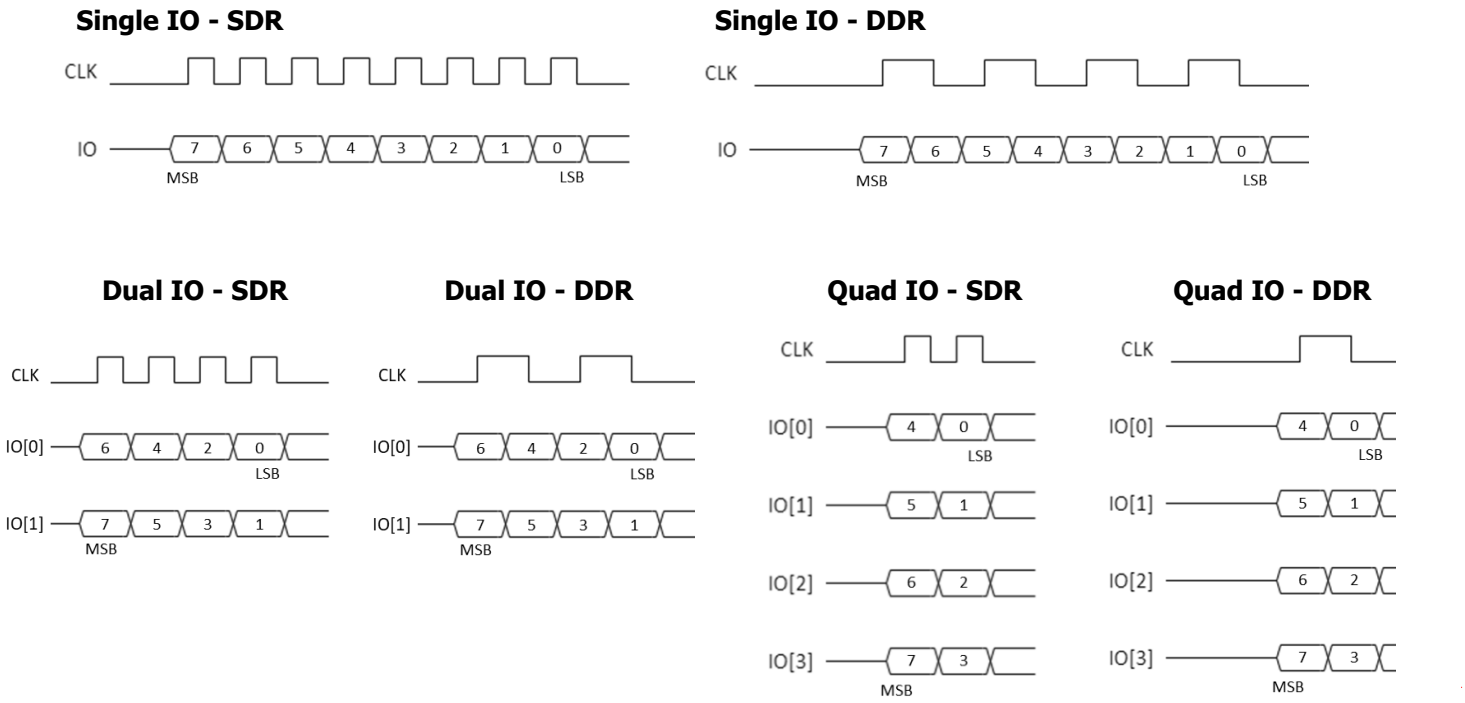
Instruction Component	Interface Modes (Command-Address-Data)						
	Extended SPI					Dual SPI	Quad SPI
	1s-1s-1s 1s-1d-1d	1s-1s-2s 1s-1d-2d	1s-2s-2s 1s-2d-2d	1s-1s-4s 1s-1d-4d	1s-4s-4s 1s-4d-4d	2s-2s-2s 2s-2d-2d	4s-4s-4s 4s-4-4d
Command	SI/IO[0]	SI/IO[0]	SI/IO[0]	SI/IO[0]	SI/IO[0]	IO[1:0]	IO[3:0]
Address	SI/IO[0]	SI/IO[0]	IO[1:0]	SI/IO[0]	IO[3:0]	IO[1:0]	IO[3:0]
Data Input	SI/IO[0]	IO[1:0]	IO[1:0]	IO[3:0]	IO[3:0]	IO[1:0]	IO[3:0]
Data Output	SO/IO[1]	IO[1:0]	IO[1:0]	IO[3:0]	IO[3:0]	IO[1:0]	IO[3:0]

Notes:
1,2 or 4 : bit width, s: SDR, d: DDR

6.3 MSB/LSB Location

The most significant bit(MSB) is placed first at all commands, address and data.

Figure 6: Location of MSB and LSB



7. Device Operation

7.1 Instruction Command Set

Each instruction begins with an 8-bit command which selects the type of operation. The command can be used independently, or followed by address and data, or followed by data only. During XIP operation, the first 24 bits represent the read or write address. Avoid entering invalid command codes (except for the following instruction sets).
The table below shows the instruction command table for each individual die.

Table 22: Instruction Command Table

Instruction Command Set		Code	Command-Address-Data						Max. Freq.
Command	Name		Extended SPI	Dual SPI	Quad SPI	XIP	Latency Cycles	Data Bytes	
Control Instructions									
No operation	NOOP	00h	1s-0-0	2s-0-0	4s-0-0	-	-	-	108MHz
Write Enable	WREN	06h	1s-0-0	2s-0-0	4s-0-0	-	-	-	108MHz
Write Disable	WRDI	04h	1s-0-0	2s-0-0	4s-0-0	-	-	-	108MHz
Enable Quad SPI	QPIE	38h	1s-0-0	2s-0-0	-	-	-	-	108MHz
Enable Dual SPI	DPIE	37h	1s-0-0	-	4s-0-0	-	-	-	108MHz
Enable Extended SPI	SPIE	FFh	-	2s-0-0	4s-0-0	-	-	-	108MHz
Enter Deep Power Down	DPDE	B9h	1s-0-0	2s-0-0	4s-0-0	-	-	-	108MHz
Exit Deep Power Down	DPDX	ABh	1s-0-0	2s-0-0	4s-0-0	-	-	-	108MHz
Software Reset Enable	SRTE	66h	1s-0-0	2s-0-0	4s-0-0	-	-	-	108MHz
Software Reset	SRST	99h	1s-0-0	2s-0-0	4s-0-0	-	-	-	108MHz
Read Register Instructions									
Read Status Register	RDSR	05h	1s-0-1s	2s-0-2s	4s-0-4s	-	-	1	108MHz
Read Configuration Register 1	RDC1	35h	1s-0-1s	2s-0-2s	4s-0-4s	-	-	1	108MHz
Read Configuration Register 2	RDC2	3Fh	1s-0-1s	2s-0-2s	4s-0-4s	-	-	1	108MHz
Read Configuration Register 3	RDC3	44h	1s-0-1s	2s-0-2s	4s-0-4s	-	-	1	108MHz
Read Configuration Register 4	RDC4	45h	1s-0-1s	2s-0-2s	4s-0-4s	-	-	1	108MHz
Read Configuration Register 1-4	RDCX	46h	1s-0-1s	2s-0-2s	4s-0-4s	-	-	4	108MHz
Read Device ID	RDID	9Fh	1s-0-1s	2s-0-2s	4s-0-4s	-	-	4	108MHz
Read Unique ID	RUID	4Ch	1s-0-1s	2s-0-2s	4s-0-4s	-	-	8	54MHz
Read Serial Number Register	RDSN	C3h	1s-0-1s	2s-0-2s	4s-0-4s	-	-	8	108MHz
Read Augmented 512-byte Protection Register	RDAP	14h	1s-0-1s	2s-0-2s	4s-0-4s	-	-	1	108MHz
Read Any Register - Address Based	RDAR	65h	1s-1s-1s	2s-2s-2s	4s-4s-4s		O	1,4,8	108MHz
Write Register Instructions									
Write Status Register	WRSR	01h	1s-0-1s	2s-0-2s	4s-0-4s	-	-	1	108MHz
Write Configuration Registers 1-4	WRCX	87h	1s-0-1s	2s-0-2s	4s-0-4s	-	-	4	108MHz
Write Serial Number Register	WRSN	C2h	1s-0-1s	2s-0-2s	4s-0-4s	-	-	8	108MHz
Write Augmented 512-byte Protection Register	WRAP	1Ah	1s-0-1s	2s-0-2s	4s-0-4s	-	-	1	108MHz
Write Any Register - Address Based	WRAR	71h	1s-1s-1s	2s-2s-2s	4s-4s-4s	-	-	1,8	108MHz

Instruction Command Set		Code	Command-Address-Data						Max. Freq.
Command	Name		Extended SPI	Dual SPI	Quad SPI	XIP	Latency Cycles	Data Bytes	
Read Memory Instructions									
Read Memory - SDR	READ	03h	1s-1s-1s	-	-	-	-	1→∞	54MHz
Fast Read Memory - SDR	RDFT	0Bh	1s-1s-1s	2s-2s-2s	4s-4s-4s	O	O	1→∞	108MHz
Fast Read Memory - DDR	DRFR	0Dh	1d-1d-1d	2s-2d-2d	4s-4d-4d	O	O	1→∞	54MHz
Read Dual Output Memory - SDR	RDDO	3Bh	1s-1s-2s	2s-2s-2s	-	O	O	1→∞	108MHz
Read Dual Output Memory - DDR	DRDO	3Dh	1s-1d-2d	2s-2d-2d	-	O	O	1→∞	54MHz
Read Dual IO Memory - SDR	RDDI	BBh	1s-2s-2s	2s-2s-2s	-	O	O	1→∞	108MHz
Read Dual IO Memory - DDR	DRDI	BDh	1s-2d-2d	2s-2d-2d	-	O	O	1→∞	54MHz
Read Quad Output Memory - SDR	RDQO	6Bh	1s-1s-4s	-	4s-4s-4s	O	O	1→∞	108MHz
Read Quad Output Memory - DDR	DRQO	6Dh	1s-1d-4d	-	4s-4d-4d	O	O	1→∞	54MHz
Read Quad IO Memory - SDR	RDQI	EBh	1s-4s-4s	-	4s-4s-4s	O	O	1→∞	108MHz
Read Quad IO Memory - DDR	DRQI	EDh	1s-4d-4d	-	4s-4d-4d	O	O	1→∞	54MHz
Write Memory Instructions									
Write Memory - SDR	WRTE	02h	1s-1s-1s	2s-2s-2s	4s-4s-4s	-	-	1→∞	108MHz
Fast Write Memory - SDR	WRFT	DAh	1s-1s-1s	2s-2s-2s	4s-4s-4s	O	-	1→∞	108MHz
Fast Write Memory - DDR	DRFW	DEh	1s-1d-1d	2s-2d-2d	4s-4d-4d	O	-	1→∞	54MHz
Write Dual Input Memory - SDR	WDUI	A2h	1s-1s-2s	2s-2s-2s	-	O	-	1→∞	108MHz
Write Dual Input Memory - DDR	DWUI	A4h	1s-1d-2d	2s-2d-2d	-	O	-	1→∞	54MHz
Write Dual IO Memory - SDR	WDIO	A1h	1s-2s-2s	2s-2s-2s	-	O	-	1→∞	108MHz
Write Dual IO Memory - DDR	DWIO	A3h	1s-2d-2d	2s-2d-2d	-	O	-	1→∞	54MHz
Write Quad Input Memory - SDR	WQDI	32h	1s-1s-4s	-	4s-4s-4s	O	-	1→∞	108MHz
Write Quad Input Memory - DDR	DWQI	31h	1s-1d-4d	-	4s-4d-4d	O	-	1→∞	54MHz
Write Quad IO Memory - SDR	WQIO	D2h	1s-4s-4s	-	4s-4s-4s	O	-	1→∞	108MHz
Write Quad IO Memory - DDR	DWQO	D1h	1s-4d-4d	-	4s-4d-4d	O	-	1→∞	54MHz
Read/Write Augmented 512-Byte Area Instructions									
Read Augmented Area	RDAS	4Bh	1s-1s-1s	-	-	-	O	1→512	108MHz
Write Augmented Area	WRAS	42h	1s-1s-1s	-	-	-	-	1→512	108MHz

Notes:
1. Cs-A(s/d)-D(s/d) format: C stands for Command input, A stands for Address input, D stands for either Data input or Output, 's' stands for SDR, 'd' stands for DDR.
   '0' in Cs-A(s/d)-D(s/d) format indicates that no byte is required.
   '-' indicates 'not supported' or 'not required'.
2. Extended SPI mode is enabled after power-on, software reset or JEDEC reset.
3. Read Register operations do not wrap data. Reading beyond the specified number of bytes will yield indeterminate data.
4. Write Enable (WREN) should be implemented in advance of Write Register Instruction set regardless of CR4[1:0] setting. The WREN prerequisite for write operation of memory and augmented area is described in Configuration Register 4.
5. Latency is configurable through Configuration Register 2 (CR2[3:0]) and frequency dependent. Required latency is described in Configuration Register 2.
6. Any other commands are not allowed.

7.2 RESET Operations

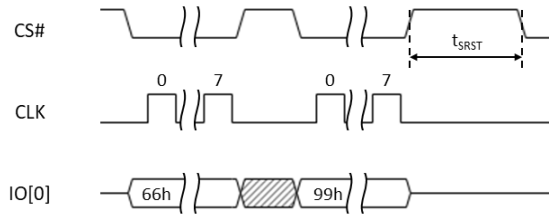
The device supports the software reset and JEDEC reset functions. The device may be reset in software by the Reset Enable and Software Reset instructions or JEDEC reset. Extended SPI mode is enabled after software reset or JEDEC reset.

7.2.1 Software Reset

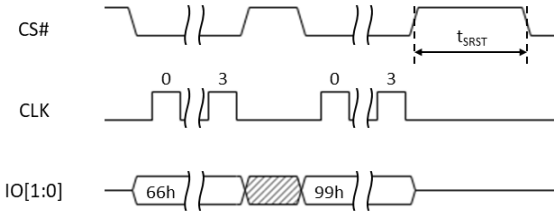
To reset the device in software, the Reset Enable command is issued, followed by the Software Reset command. The device then enters a power-on reset condition. The CS# High time(t_{SRST}) must be observed between commands.

Figure 7: Software Reset Timing

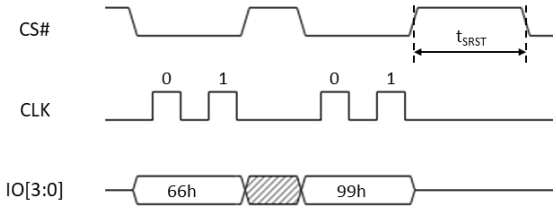
Extended SPI



Dual SPI



Quad SPI



7.2.2 JEDEC Reset

Figure 8: JEDEC Reset Timing

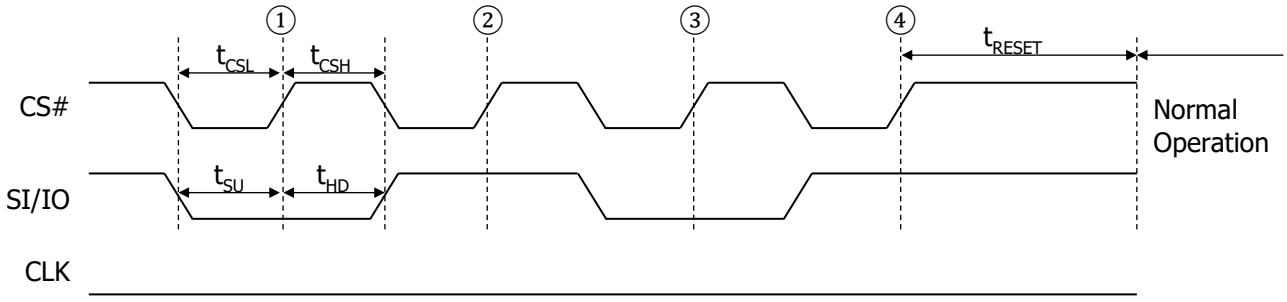


Table 23: JEDEC Reset Timing

Parameter	Symbol	Min.	Max.	Units
CS# Low Time	t_{CSL}	0.5	-	µs
CS# High Time	t_{CSH}	0.5	-	µs
SI/IO[0] Setup Time (w.r.t CS#)	t_{SU}	5.0	-	ns
SI/IO[0] Hold Time (w.r.t CS#)	t_{HD}	5.0	-	ns
JEDEC Hardware Reset (3.3V)	t_{RESET}	-	0.3	ms
JEDEC Hardware Reset (1.8V)	t_{RESET}	-	2.0	ms

7.3 WRITE ENABLE/DISABLE Operations

To initiate a command for each die, CS# must be driven Low and held Low until the eighth bit of the command code is latched in, then driven High. For Extended SPI, Dual SPI and Quad SPI protocols respectively, the command code is input on IO[0], IO[1:0] and IO[3:0].
A Write Enable command (WREN) is needed to set the WREN bit prior to Write Register Instruction regardless of CR4[1:0] setting.
The WREN prerequisite for write operation of memory and augmented area is described in Configuration Register 4.

Figure 9: WRITE Enable/Disable Timing

WRITE ENABLE (06h) **WRITE DISABLE (04h)**

Extended SPI

Dual SPI

Quad SPI

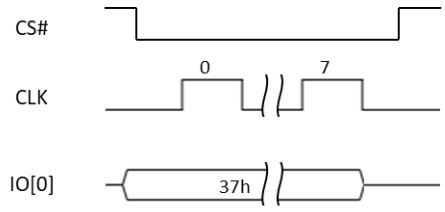
7.4 Enable Extended, Dual and Quad SPI mode

To initiate a command for each die, CS# is driven Low and held Low until the eighth bit of the command code is latched in, then driven High. For Extended SPI, Dual SPI and Quad SPI protocols respectively, the command code is input on IO[0], IO[1:0] and IO[3:0].

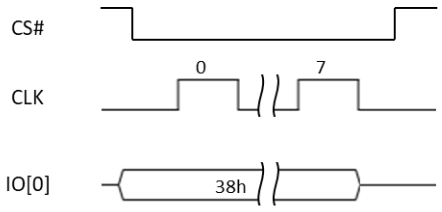
When Quad SPI is enabled, CR2[6] bit of the Configuration Register 2 is set to '1' and when Dual SPI is enabled, CR2[4] bit of the Configuration Register 2 is set to '1'.

Figure 10: Enable Extended SPI or Quad SPI mode

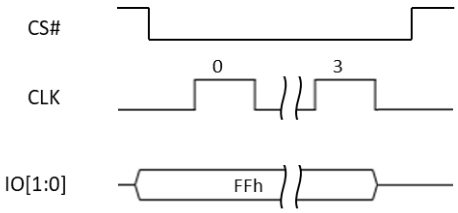
Extended SPI ➔ Dual SPI



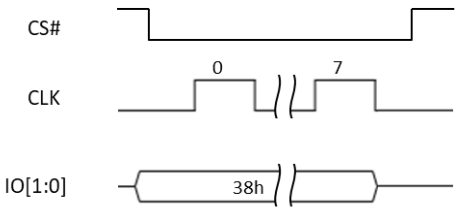
Extended SPI ➔ Quad SPI



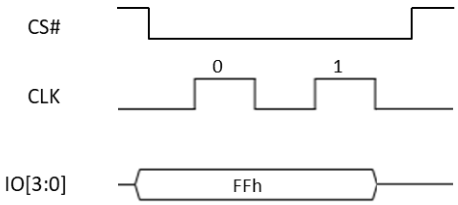
Dual SPI ➔ Extended SPI



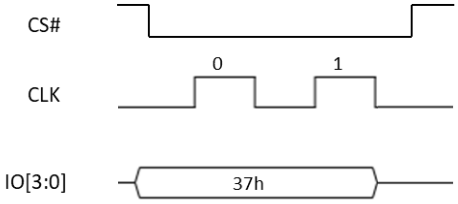
Dual SPI ➔ Quad SPI



Quad ➔ Extended SPI



Quad SPI ➔ Dual SPI



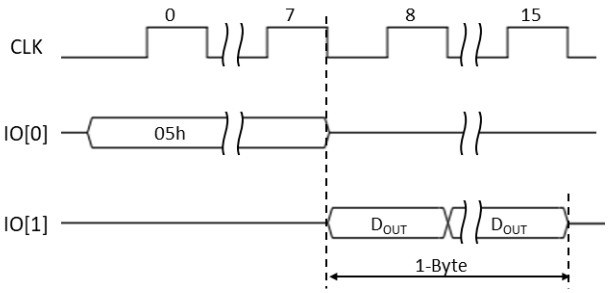
7.5 Register Operation

7.5.1. Read Register Operations

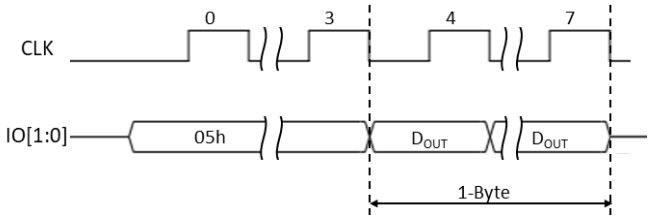
To initiate register read operations, CS# is driven Low and the command code is input, followed by input of the address bytes if required. The operation is terminated by driving CS# High, and the output goes to High-Z.

Figure 11: Read Status Register Timing

Extended SPI



Dual SPI



Quad SPI

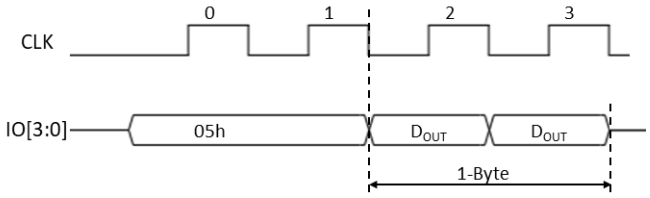
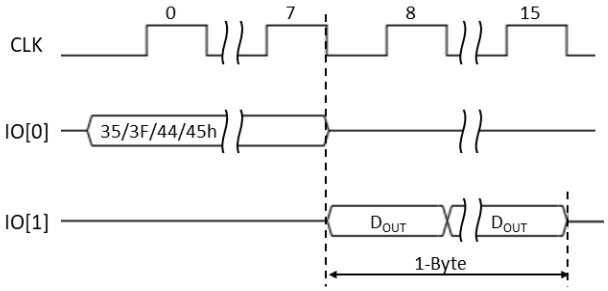
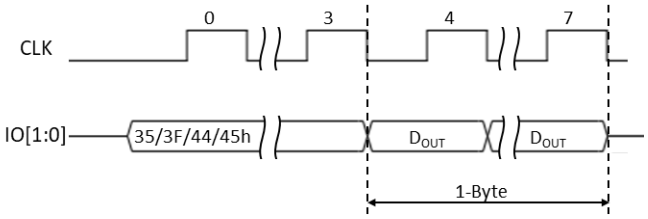


Figure 12: Read Configuration Register 1, 2, 3 or 4 Timing

Extended SPI



Dual SPI



Quad SPI

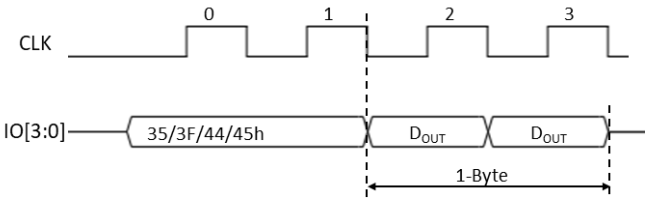
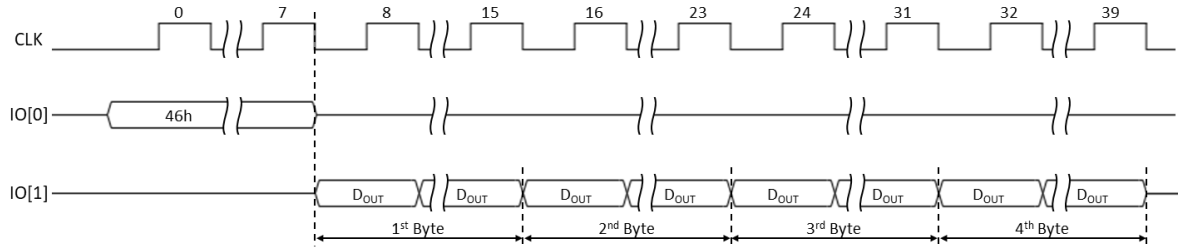
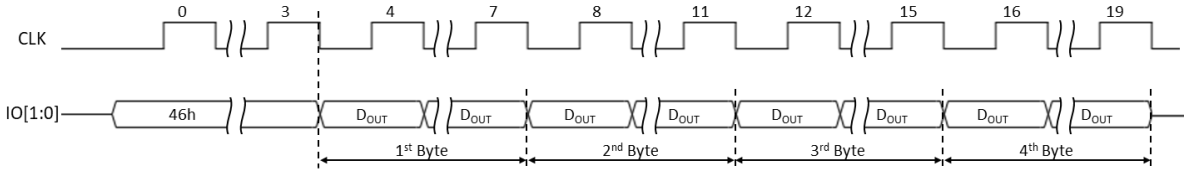


Figure 13: Read Configuration Register 1-4 Timing

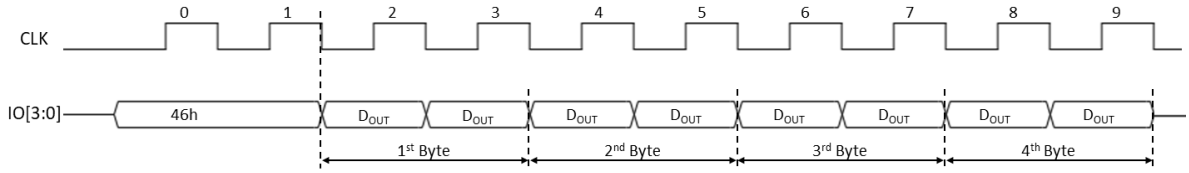
Extended SPI



Dual SPI



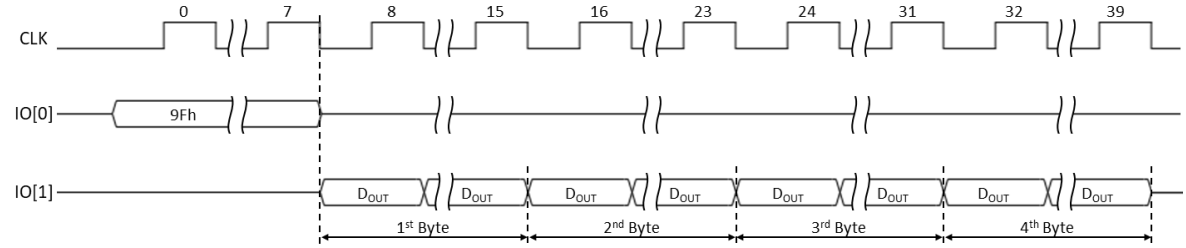
Quad SPI



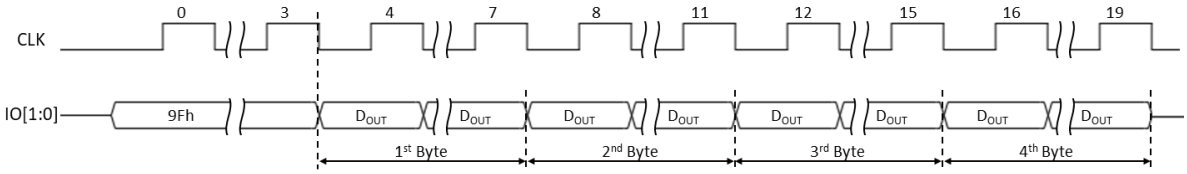
Notes: 1st Byte: CR1[7:0], 2nd Byte: CR2[7:0], 3rd Byte: CR3[7:0], 4th Byte: CR4[7:0],

Figure 14: Read Device ID Timing

Extended SPI



Dual SPI



Quad SPI

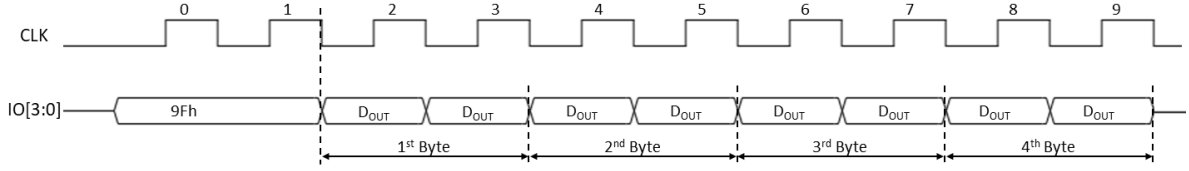
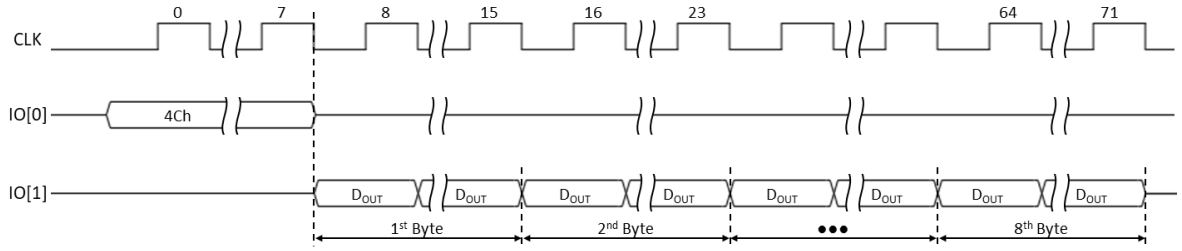
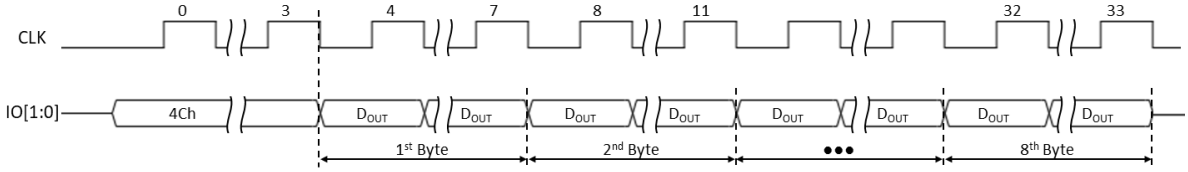


Figure 15: Read Unique ID Timing

Extended SPI



Dual SPI



Quad SPI

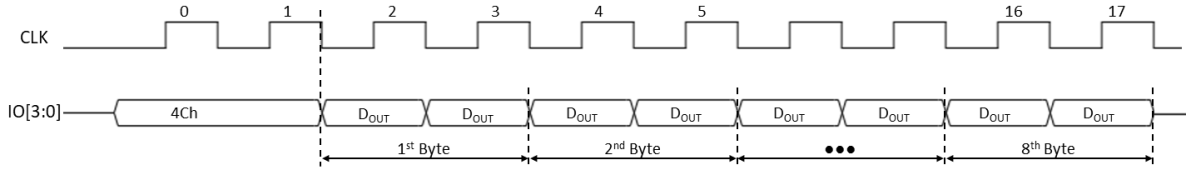
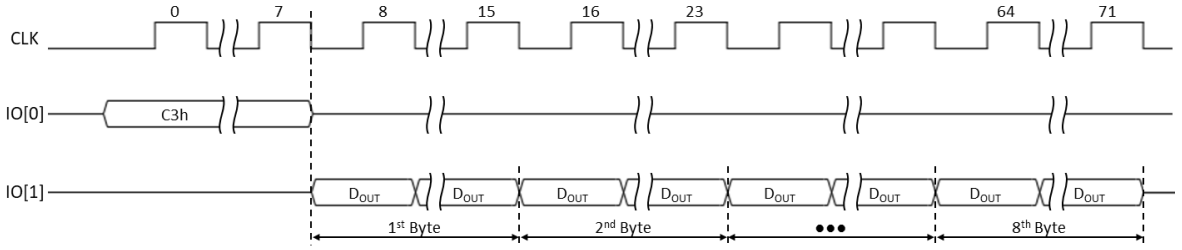
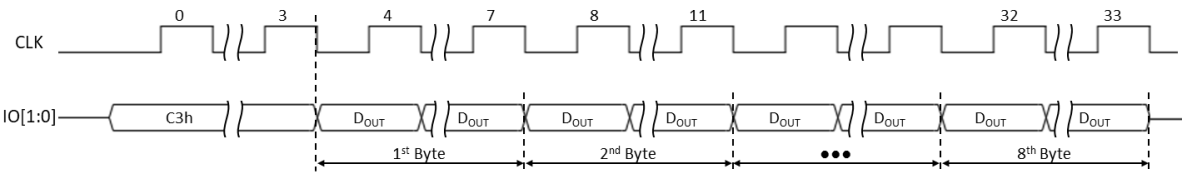


Figure 16: Read Serial Number Register Timing

Extended SPI



Dual SPI



Quad SPI

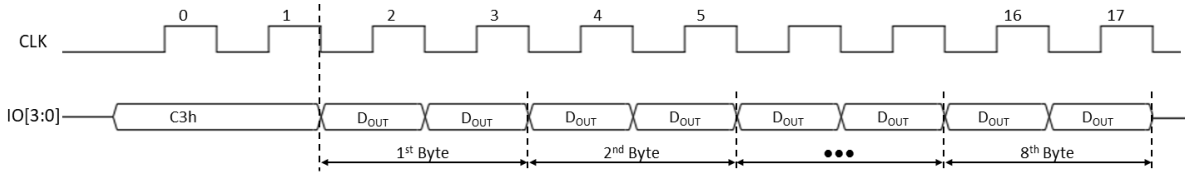
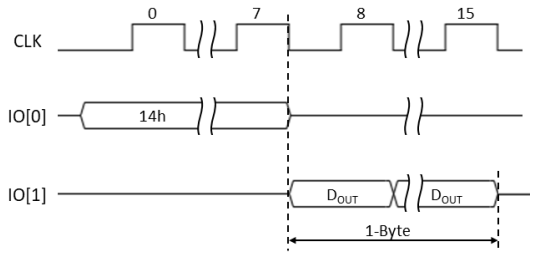
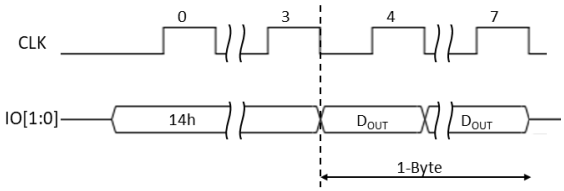


Figure 17: Read Augmented 512-byte Protection Register Timing

Extended SPI



Dual SPI



Quad SPI

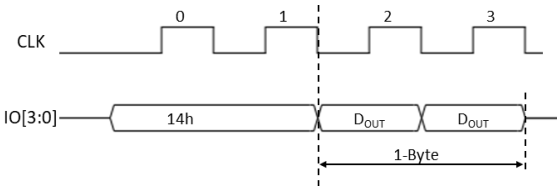
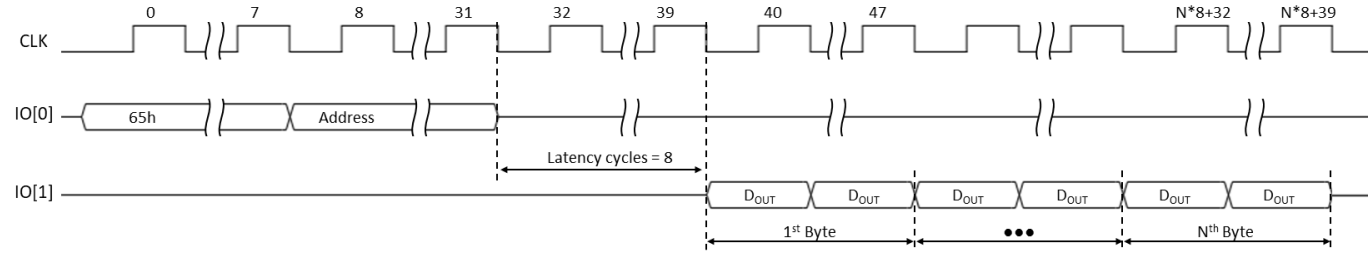
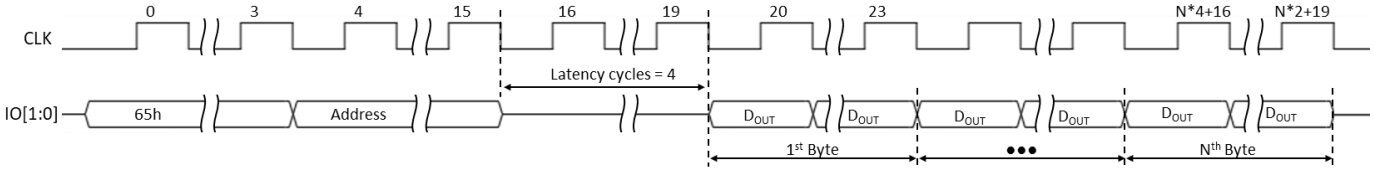


Figure 18: Read Any Register Timing

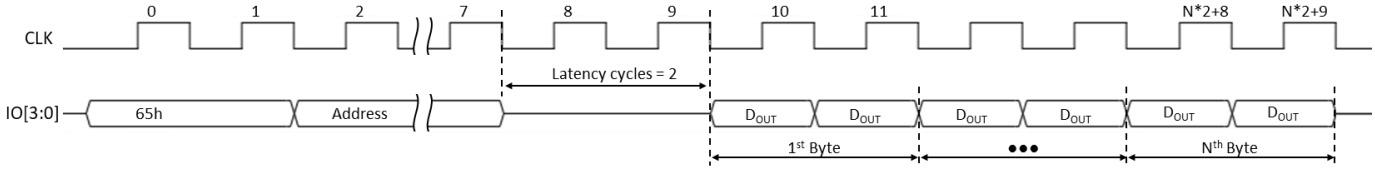
Extended SPI



Dual SPI



Quad SPI



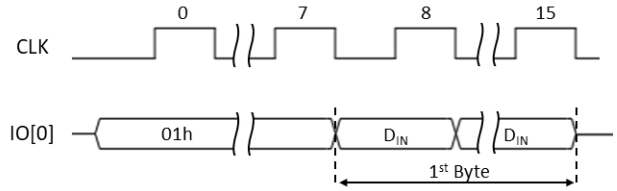
Notes:
1. The latency cycles of Read Any Register instruction (65h) are 8 in Extended SPI, 4 in Dual SPI or 2 in Quad SPI, regardless of Read latency Selection Bits CR2[3:0].
2. N can be 1, 4, or 8. See the table 6 - Register Address Map.

7.5.2. WRITE REGISTER Operations

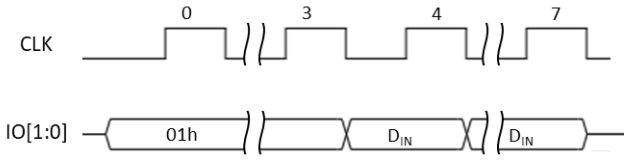
Before a Write Register command is initiated, Status Register or Configuration Register should be set Writable (See Table 8: Write Protection Modes).
To initiate register write operations, CS# is driven Low and the command code is input, followed by input of the address bytes if required, and followed by the input data. The operation is terminated by driving CS# High.

Figure 19: Write Status Register Timing

Extended SPI



Dual SPI



Quad SPI

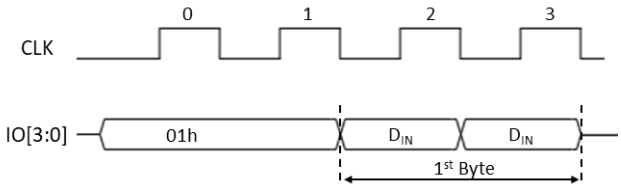
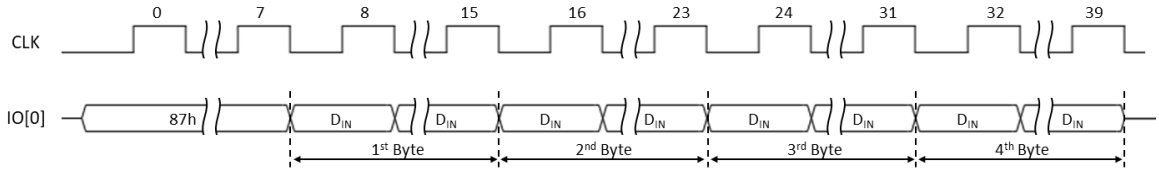
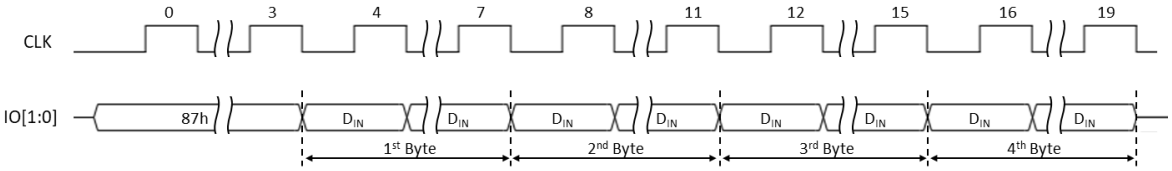


Figure 20: Write Configuration Register 1-4 Timing

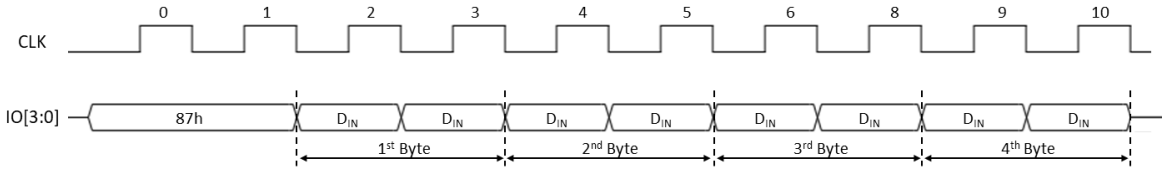
Extended SPI



Dual SPI



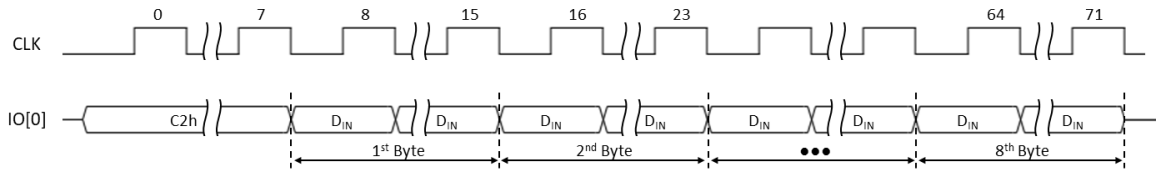
Quad SPI



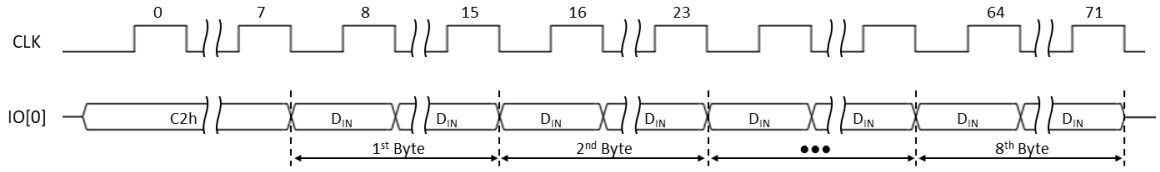
Notes: 1st Byte: CR1[7:0], 2nd Byte: CR2[7:0], 3rd Byte: CR3[7:0], 4th Byte: CR4[7:0],

Figure 21: Write Serial Number Register Timing

Extended SPI



Dual SPI



Quad SPI

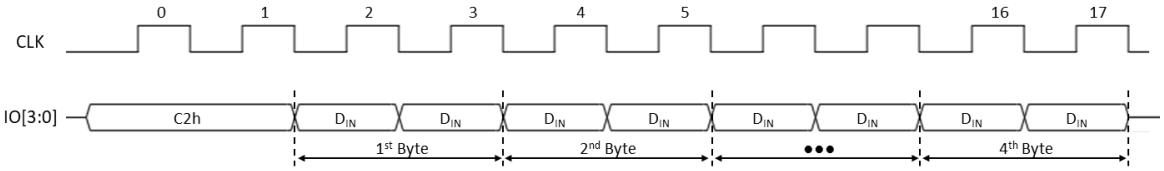
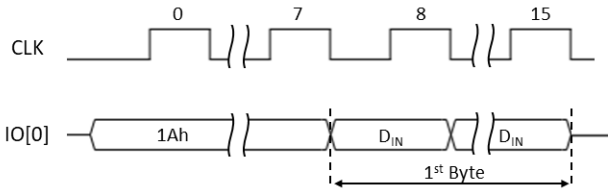
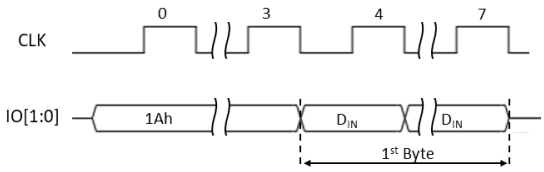


Figure 22: Write Augmented 512-byte Protection Register Timing

Extended SPI



Dual SPI



Quad SPI

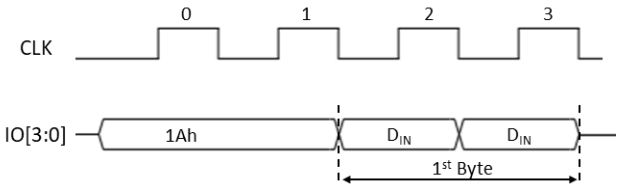
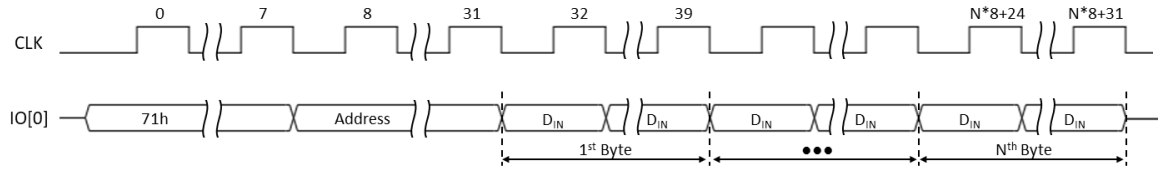
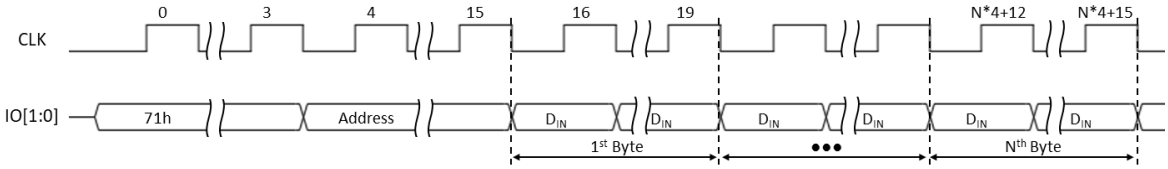


Figure 23: Write Any Register Timing

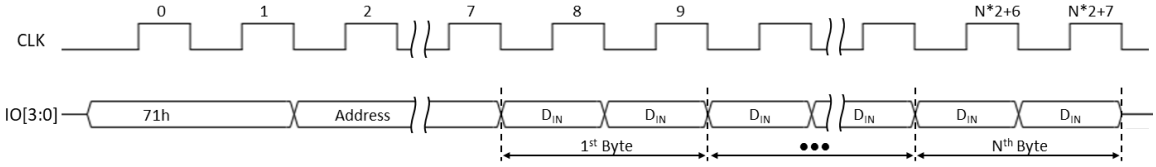
Extended SPI



Dual SPI



Quad SPI



Notes:
1. N can be 1 or 8 depending on the address. See the table 6 - Register Address Map

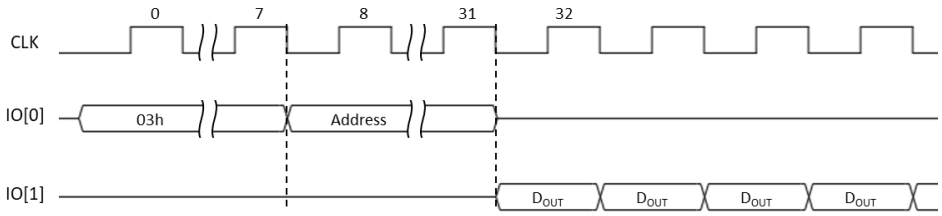
7.6 Memory Operation

To initiate memory read operation, CS# is driven Low and the command code is input, followed by input of the address bytes. The operation is terminated by driving CS# High at any time during data output.

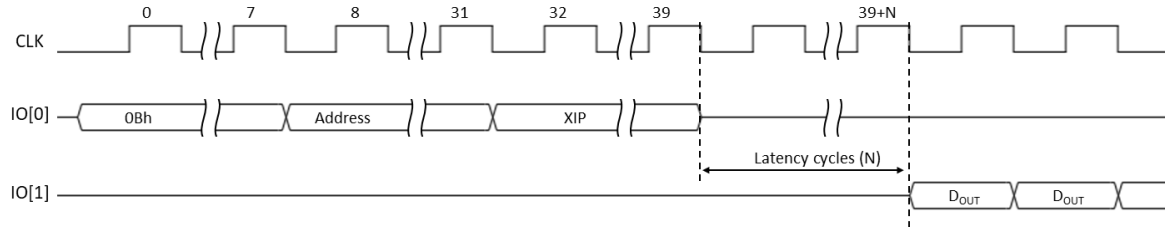
7.6.1 READ MEMORY Operations

Figure 24: Read Memory Timing

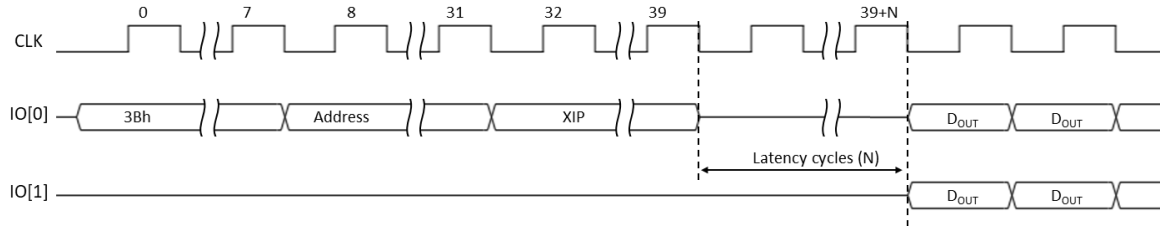
1) 1s-1s-1s transaction
Extended SPI: Read Memory (03h)



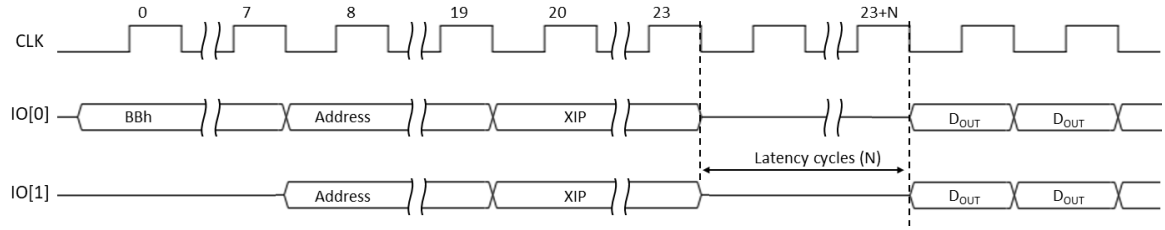
2) 1s-1s-1s transaction
Extended SPI: Fast Read Memory (0Bh)



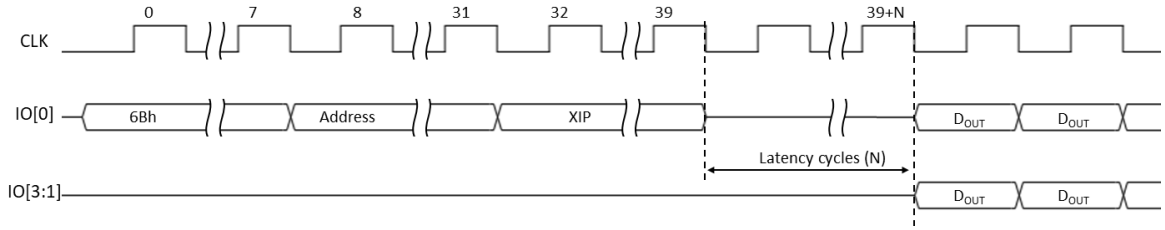
3) 1s-1s-2s transaction
Extended SPI: Read Dual Output Memory (3Bh)



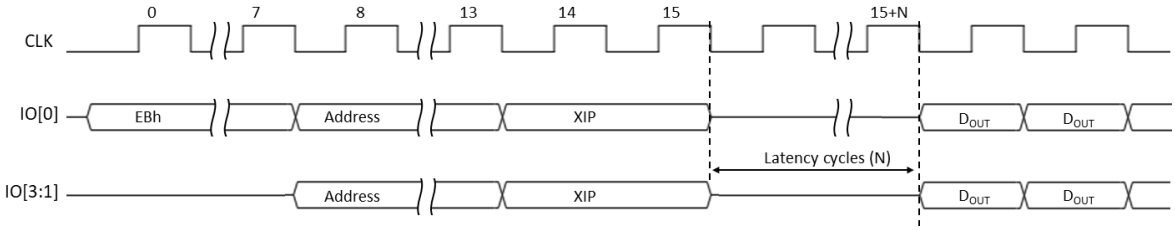
4) 1s-2s-2s transaction
Extended SPI: Read Dual IO Memory (BBh)



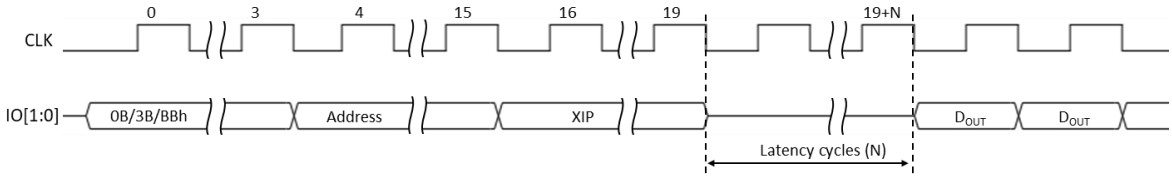
5) 1s-1s-4s transaction
Extended SPI: Read Quad Output Memory (6Bh)



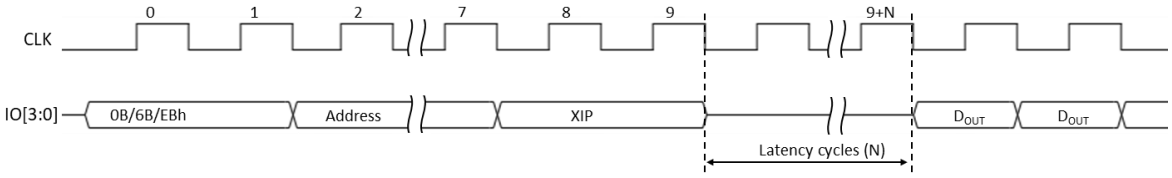
6) 1s-4s-4s transaction
Extended SPI: Read Quad IO Memory (EBh)



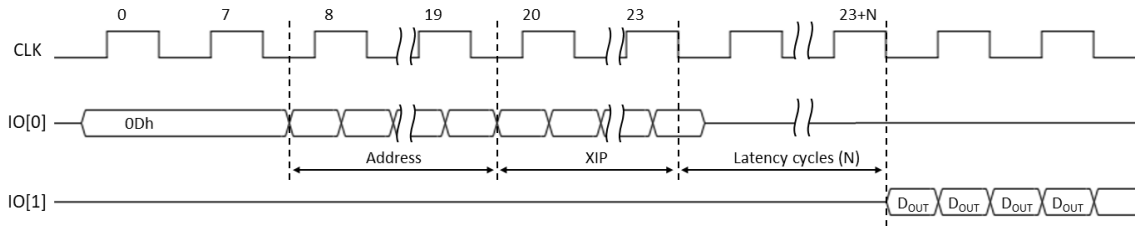
7) 2s-2s-2s transaction
Dual SPI: Fast Read Memory (0Bh), Read Dual Output Memory (3Bh), Read Dual IO Memory (BBh)



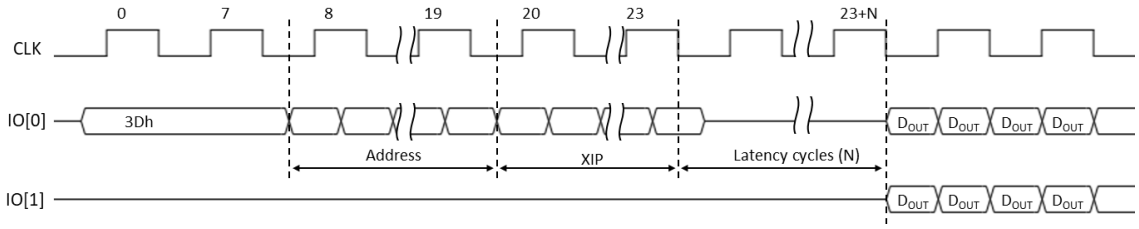
8) 4s-4s-4s transaction
Quad SPI: Fast Read Memory (0Bh), Read Quad Output Memory (6Bh), Read Quad IO Memory (EBh)



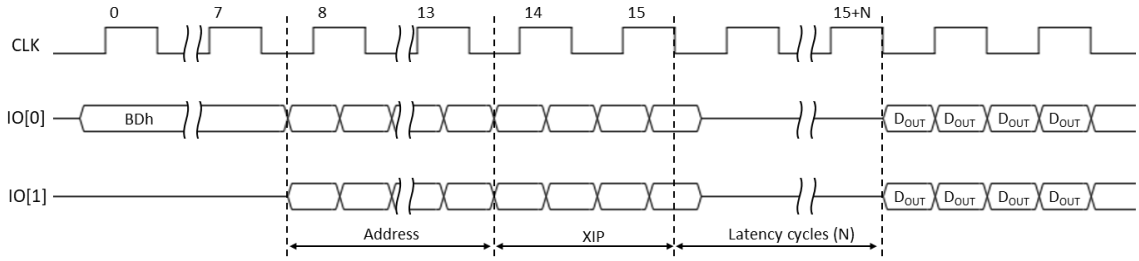
9) 1s-1d-1d transaction
Extended SPI: Fast Read Memory-DDR (0Dh)



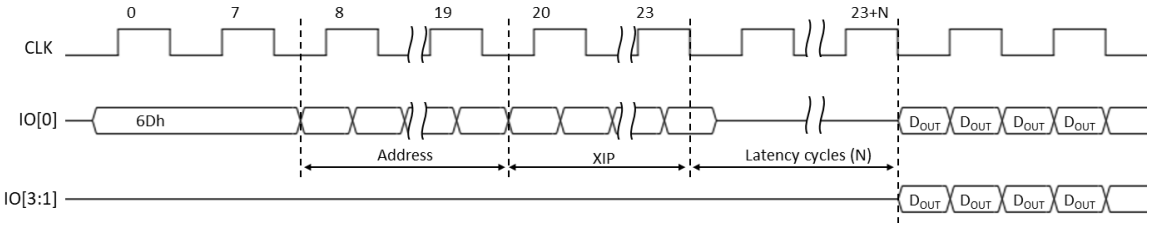
10) 1s-1d-2d transaction
Extended SPI: Read Dual Output Memory-DDR DDR (3Dh)



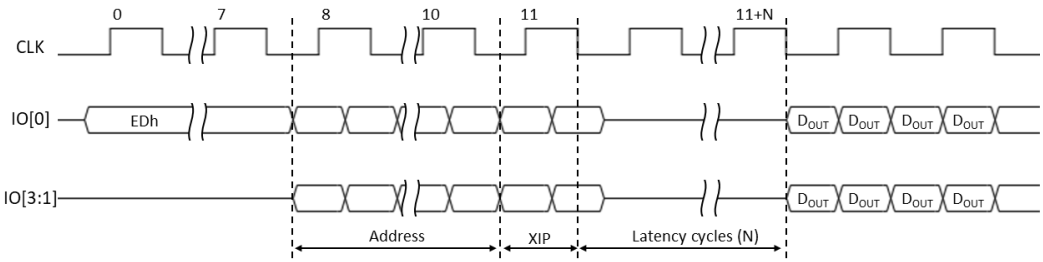
11) 1s-2d-2d transaction
Extended SPI: Read Dual IO Memory-DDR DDR (BDh)



12) 1s-1d-4d transaction
Extended SPI: Read Quad Output Memory-DDR (6Dh)

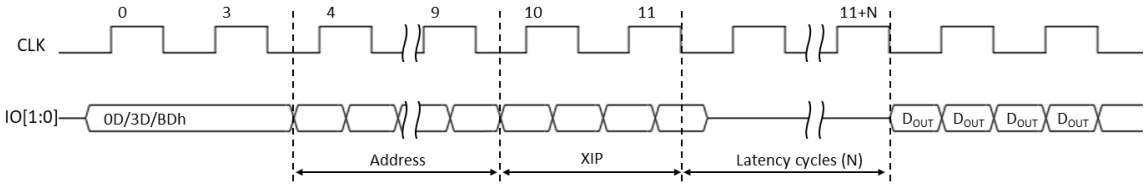


13) 1s-4d-4d transaction
Extended SPI: Read Quad IO Memory-DDR (EDh)



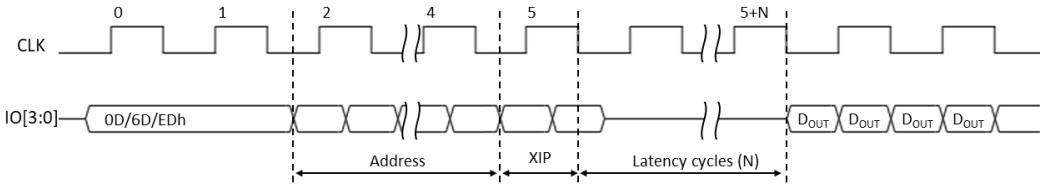
14) 2s-2d-2d transaction

Dual SPI: Fast Read Memory-DDR (0Dh), Read Dual Output Memory-DDR (3Dh), Read Dual IO Memory -DDR (BDh)



15) 4s-4d-4d transaction

Quad SPI: Fast Read Memory-DDR (0Dh), Read Quad Output Memory-DDR (6Dh), Read Quad IO Memory -DDR (EDh)

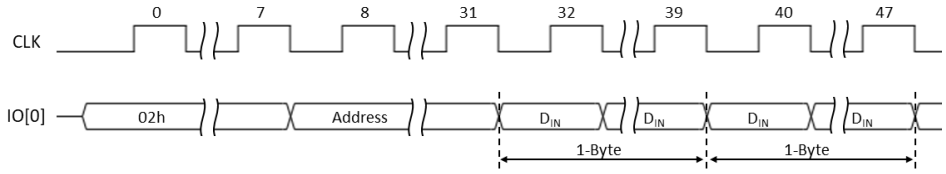


7.6.2 Write Memory Operations

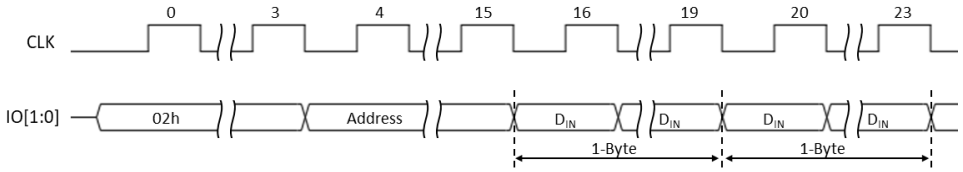
To initiate memory write operation, CS# is driven Low and the command code is input, followed by input of the address and data. The operation is terminated by driving CS# High at any time during data input. The WREN prerequisite for write operation of memory is described in Configuration Register 4.

Figure 25: Write Memory Timing

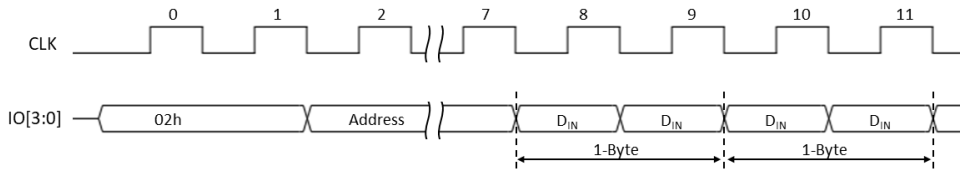
1) 1s-1s-1s transaction
Extended SPI: Write Memory (02h)



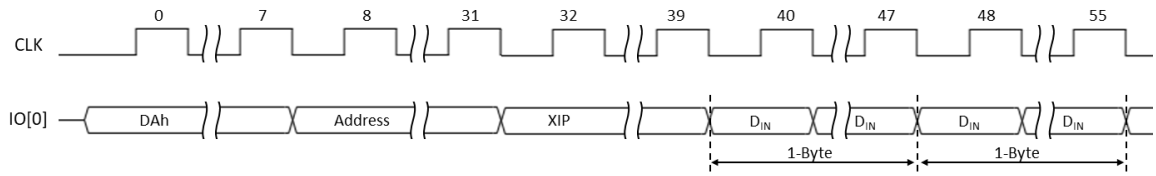
2) 2s-2s-2s transaction
Dual SPI: Write Memory (02h)



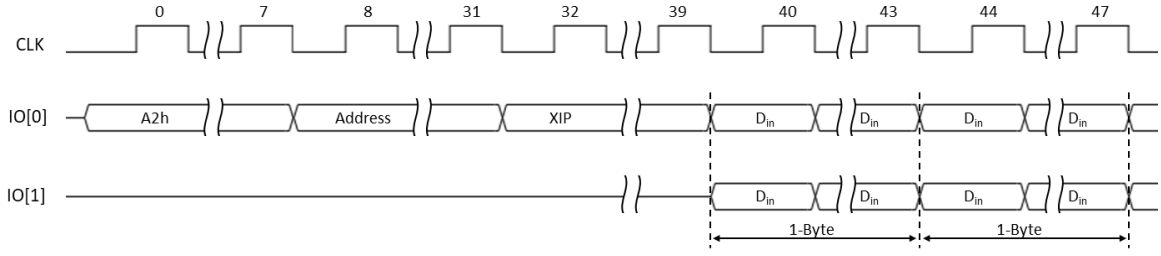
3) 4s-4s-4s transaction
Quad SPI: Write Memory (02h)



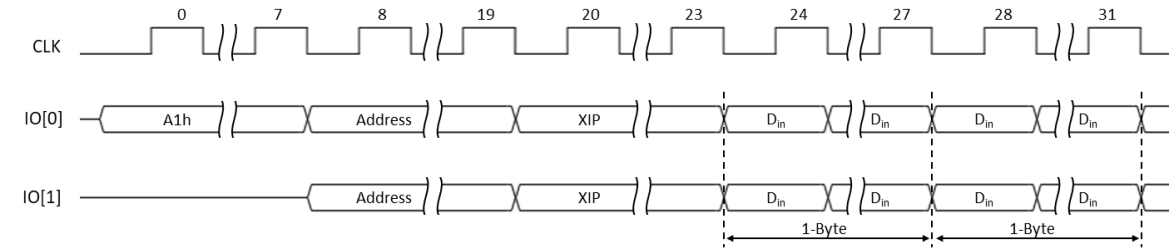
4) 1s-1s-1s transaction with XIP
Extended SPI: Fast Write Memory (DAh)



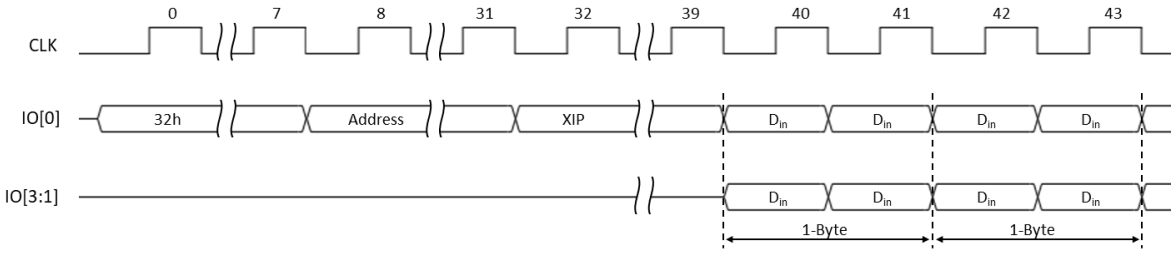
5) 1s-1s-2s transaction with XIP
Extended SPI: Write Dual Input Memory (A2h)



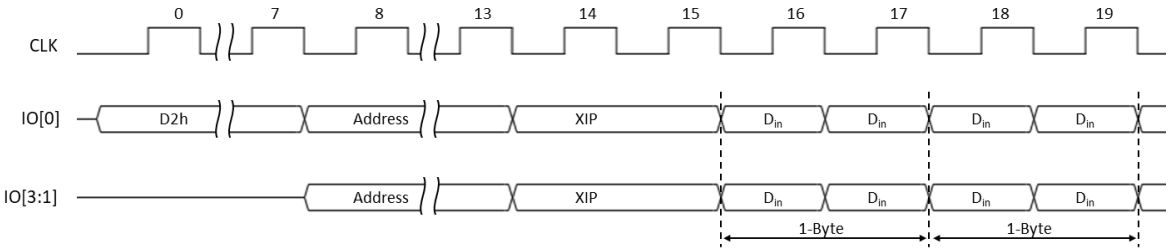
6) 1s-2s-2s transaction with XIP
Extended SPI: Write Quad I/O Memory (A1h)



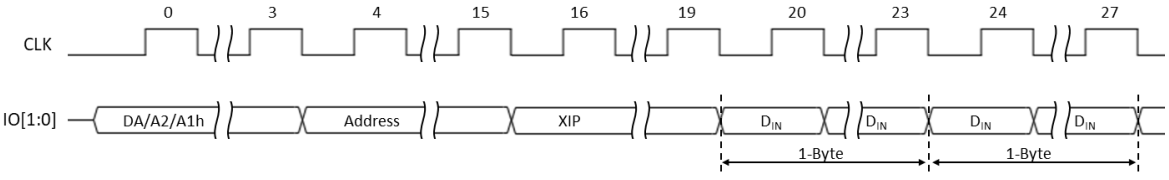
7) 1s-1s-4s transaction with XIP
Extended SPI: Write Quad Input Memory (32h)



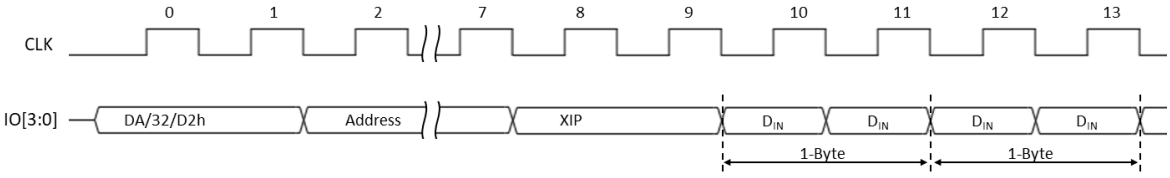
8) 1s-4s-4s transaction with XIP
Extended SPI: Write Quad IO Memory (D2h)



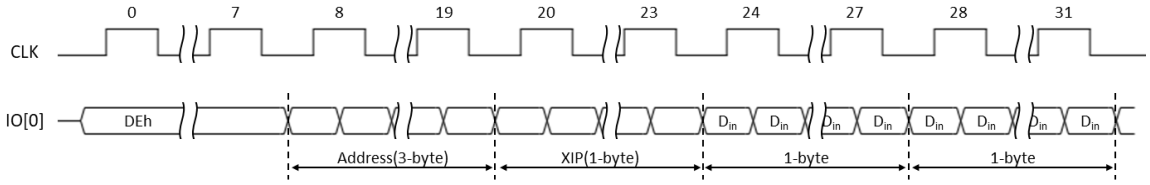
9) 2s-2s-2s transaction with XIP
Dual SPI: Fast Write Memory (DAh), Write Dual Input Memory (A2h), Write Dual IO Memory (A1h)



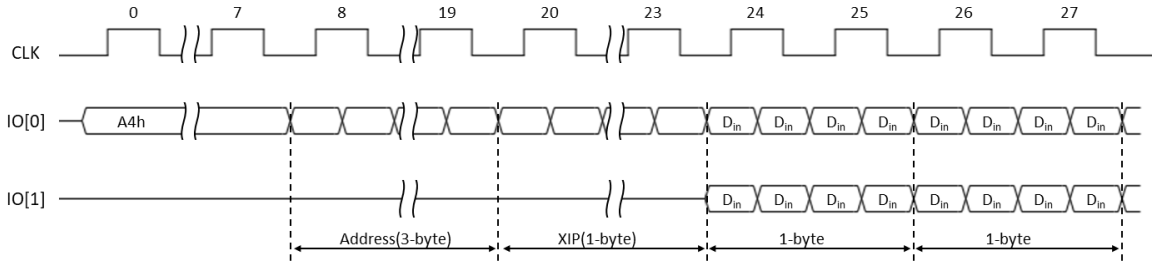
10) 4s-4s-4s transaction with XIP
Quad SPI: Fast Write Memory (DAh), Write Quad Input Memory (32h), Write Quad IO Memory (D2h)



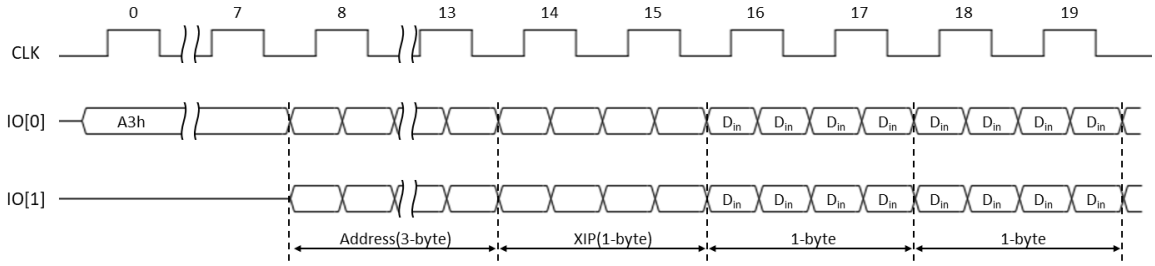
11) 1s-1d-1d transaction with XIP
Extended SPI: Fast Write Memory -DDR (DEh)



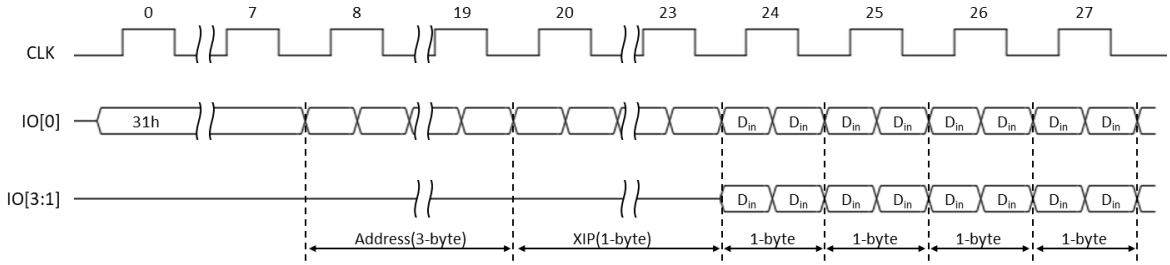
12) 1s-1d-2d transaction with XIP
Extended SPI: Write Dual Input Memory -DDR (A4h)



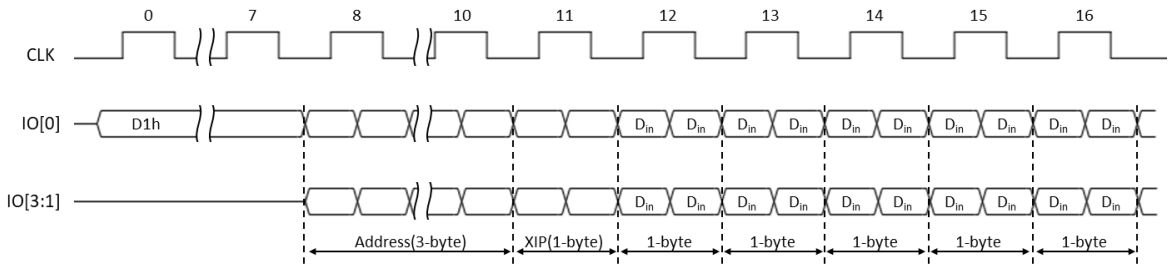
13) 1s-2d-2d transaction with XIP
Extended SPI: Write Dual IO Memory -DDR (A3h)



14) 1s-1d-4d transaction with XIP
Extended SPI: Write Quad Input Memory -DDR (31h)

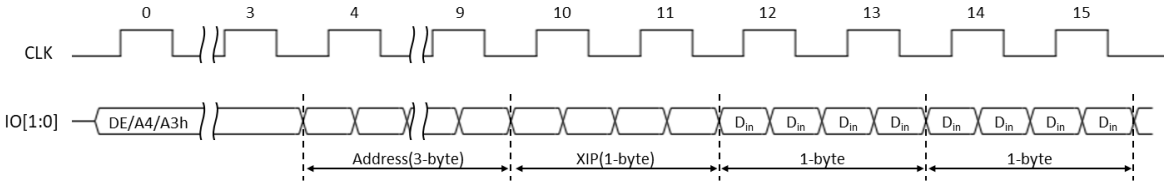


15) 1s-4d-4d transaction with XIP
Extended SPI: Write Quad IO Memory -DDR (D1h)



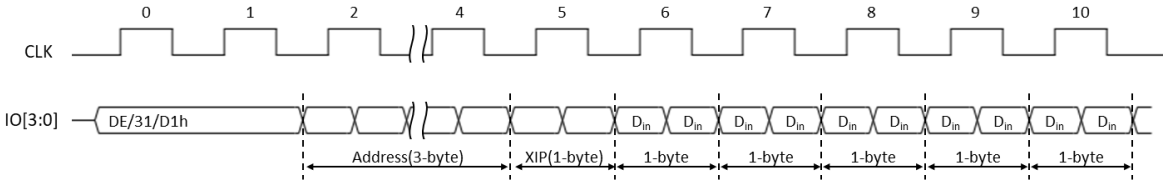
16) 2s-2d-2d transaction with XIP

Dual SPI: Fast Write Memory -DDR(DEh), Write Dual Input Memory -DDR(A4h), Write Dual IO Memory -DDR (A3h)



17) 4s-4d-4d transaction with XIP

Quad SPI: Fast Write Memory -DDR(DEh), Write Quad Input Memory -DDR(31h), Write Quad IO Memory -DDR (D1h)



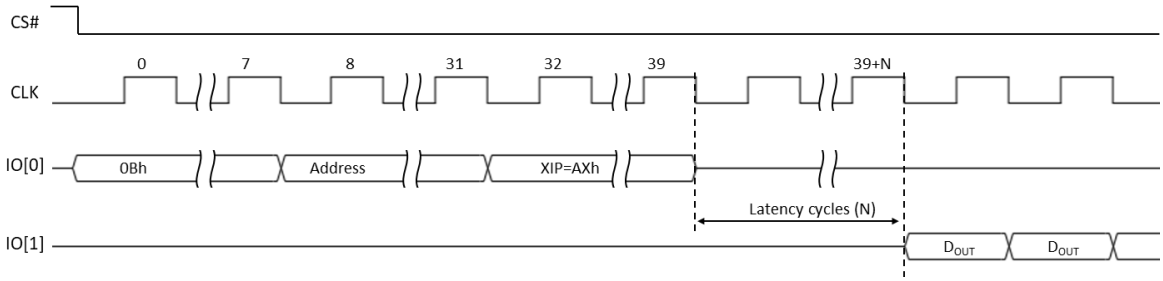
7.6.3 XIP Operations

The device offers XIP (execute in place) mode for both read and write operations.
XIP allows a series of read or write operation without loading individual read or write command for each instruction, which results in reduced random access time. XIP is enabled by entering byte AXh and disabled by entering any byte not equal to AXh (X=Don't Care). These respective bytes must be entered following the address bits. Read operation with XIP needs extra read latency cycles before data output. The read latency cycles are specified in Table 12.

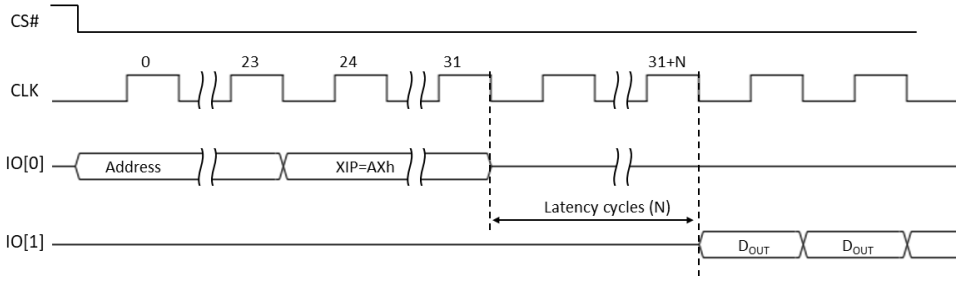
Figure 26: Read XIP Timing

1)1s-1s-1s transaction, Extended SPI, Read operation

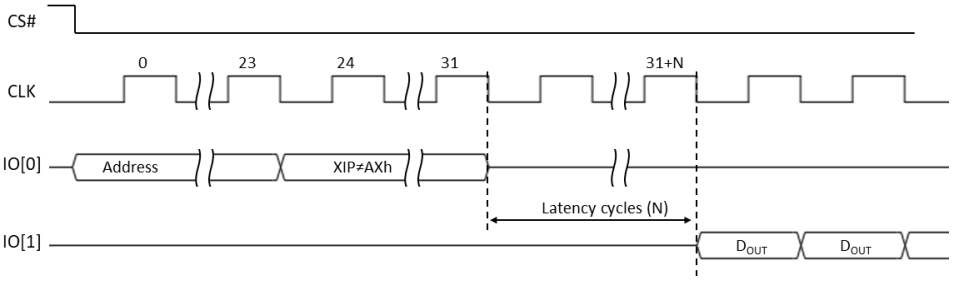
- **Enabling XIP**



- **Continuous XIP**

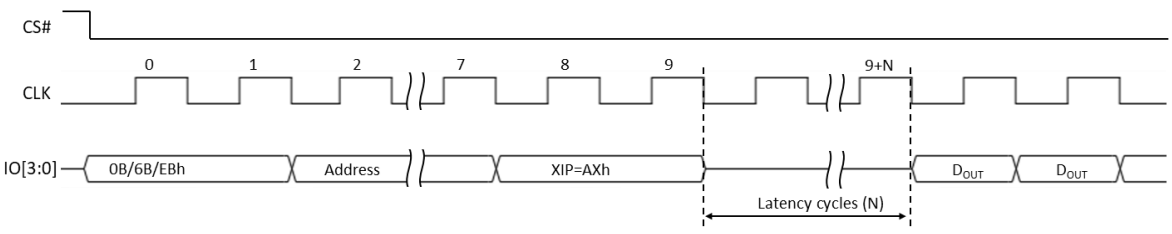


- **Terminating XIP**

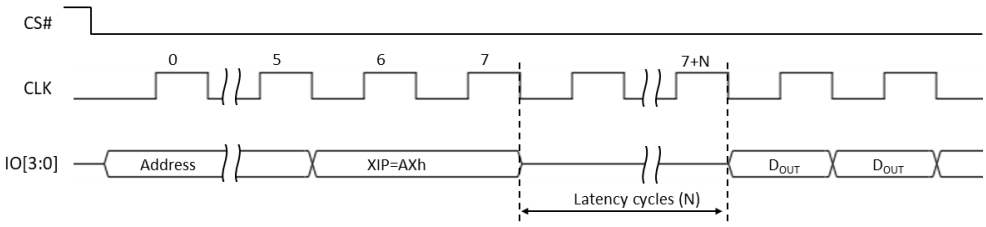


2)4s-4s-4s transaction, Quad SPI, Read operation

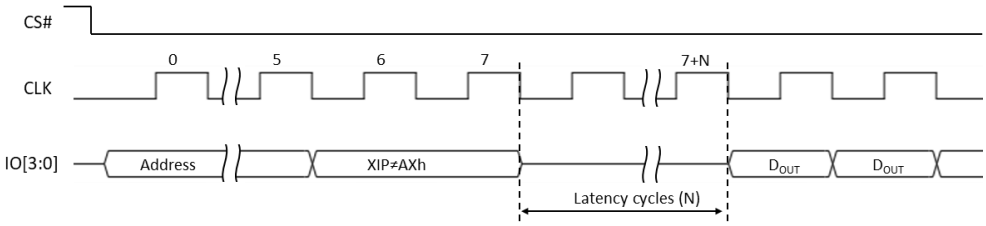
- **Enabling XIP**



- **Continuous XIP**

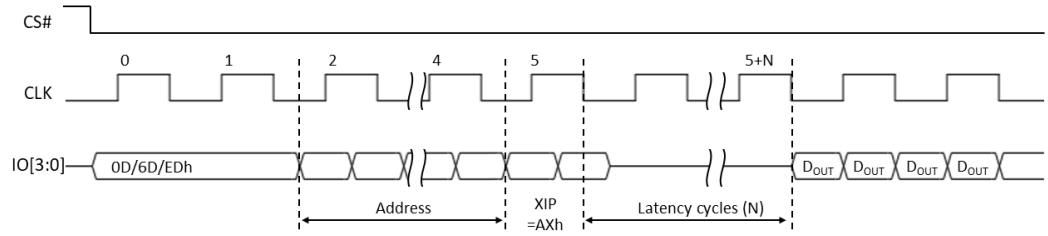


- **Terminating XIP**

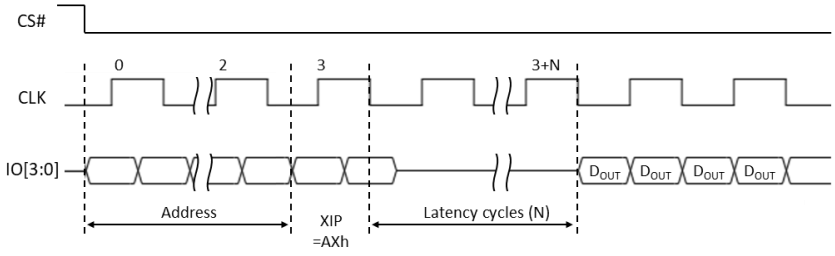


3)4s-4d-4d transaction, Quad SPI, Read operation

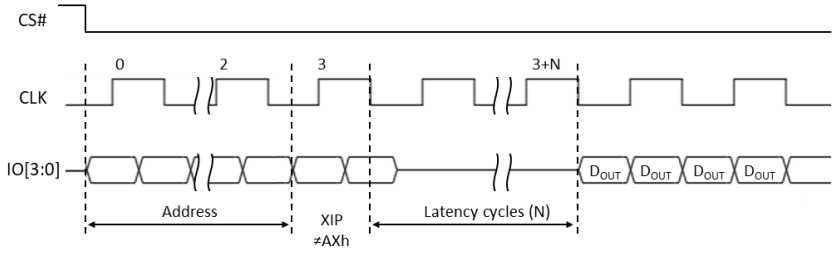
- **Enabling XIP**



- **Continuous XIP**



- **Terminating XIP**



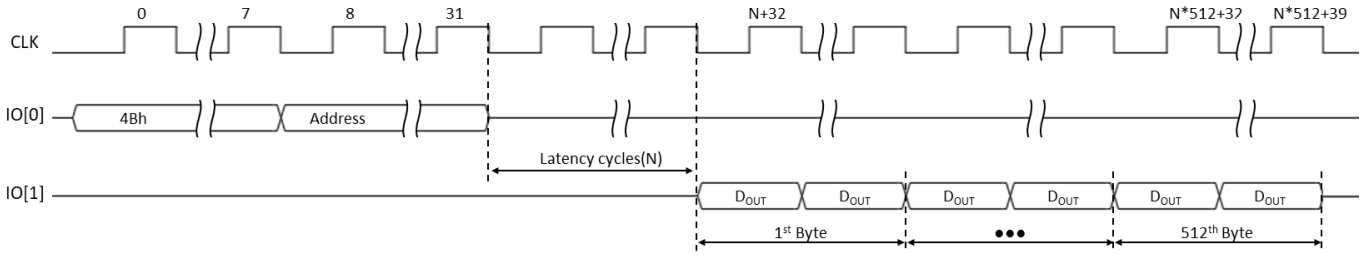
Other transactions or Write XIP operations are similar.

7.7 Augmented Area Operation

To initiate read operation for augmented area, CS# is driven Low and the command code is input, followed by input of the address bytes. The operation is terminated by driving CS# High at any time during data output.

Figure 27: Read Augmented 512-byte Area Timing

1s-1s-1s transaction

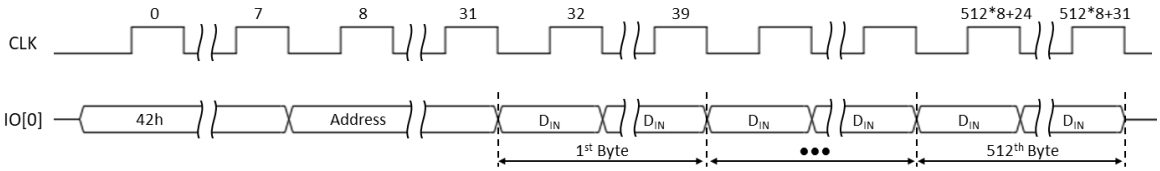


Notes:
1. Latency cycles for Read Augmented 512-byte Area are configurable through Configuration Register 2 (CR2[3:0]).

To initiate write operation for augmented area, CS# is driven Low and the command code is input, followed by input of the address and data. The operation is terminated by driving CS# High at any time during data input. The WREN prerequisite for write operation of augmented area is described in Configuration Register 4.

Figure 28: Write Augmented 512-byte Area Timing

1s-1s-1s transaction

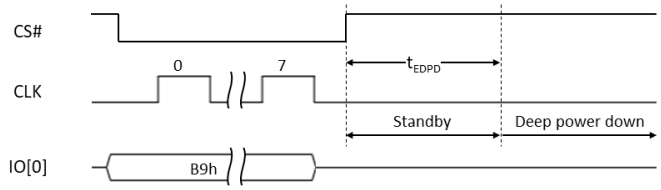


7.8 Deep Power-down Operation

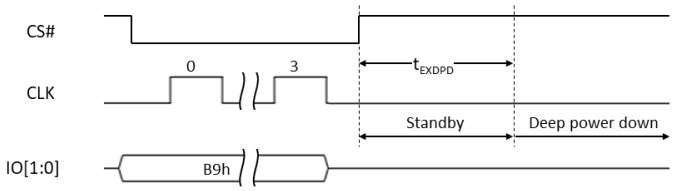
The device provides Deep Power Down mode. This mode reduces current consumption from I_{SB} to I_{DPD}. To enter the deep power down mode, CS# is driven Low, followed by Enter Deep Power Down (B9h) command, CS# is driven High after the eighth bit of the command code has been latched in.
After CS# is driven High, it requires a delay of t_{EDPD} before the supply current is reduced to I_{DPD} and the Deep Power Down mode is entered. The command can be issued in Extended SPI or Quad SPI modes.

Deep Power-down Enter

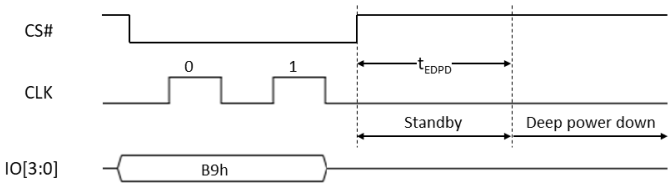
Extended SPI



Dual SPI



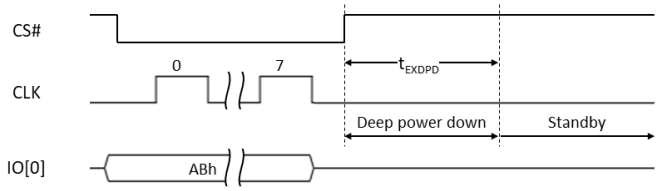
Quad SPI



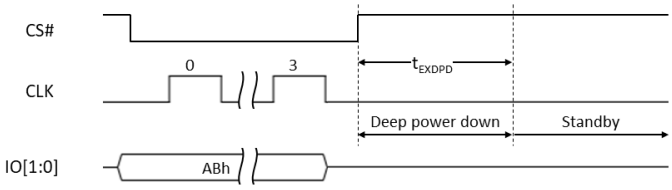
There are two ways to exit deep power down mode:
1. Driving CS# Low is followed with Exit Deep Power Down (ABh) command. CS# must be driven High after the eight bit of the command code is latched in.
2. Toggling CS# with a pulse width of t_{CSDPD} while CLK and I/Os are Don't Care state. During waking up from deep power down, I/Os remain to be in High-Z.

Deep Power-down Exit

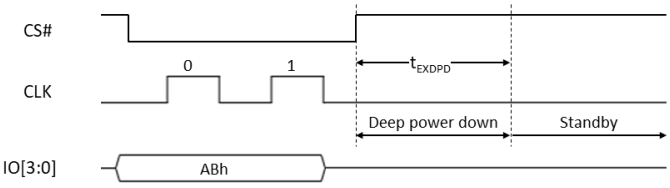
Extended SPI



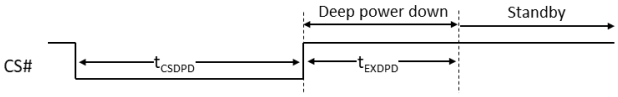
Dual SPI



Quad SPI



Toggling CS#



It requires a delay of t_{EXDPD} before the device can fully exit the deep power down mode and enter standby mode.
Status of all non-volatile bits in registers and operation mode (Extended or Quad SPI mode) remains unchanged when the device enters or exits the deep power down mode. The command can be issued in Extended SPI or Quad SPI mode.

7.9 Multi-Die Operation

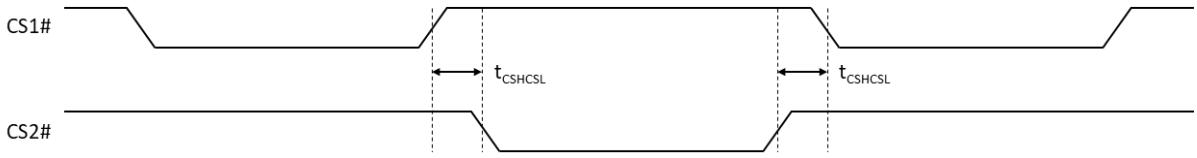
7.9.1 Chip Select Operation

In all read operations and write operations for memory and augmented 512-byte area, both CS1# and CS2# are not allowed to be active Low simultaneously. However, for Control instructions and Write Register instructions, they can be allowed to be active low simultaneously to input the same instructions or write the same data to registers.

Control Instructions	
No operation	00h
Write Enable	06h
Write Disable	04h
Enable Quad SPI	38h
Enable Dual SPI	37h
Enable Extended SPI	FFh
Enter Deep Power Down	B9h
Exit Deep Power Down	ABh
Software Reset Enable	66h
Software Reset	99h

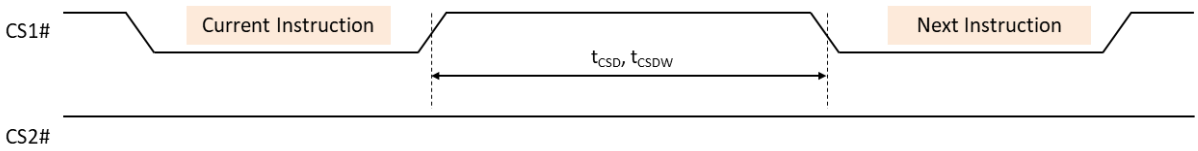
Write Register Instructions	
Write Status Register	01h
Write Configuration Registers 1-4	87h
Write Serial Number Register	C2h
Write Augmented 512-byte Protection Register	1Ah
Write Any Register - Address Based	71h

The time minimum interval time (t_{CSHCSL}) between CS1# (or CS2#) going High and CS2# (orCS1#) going Low is 0ns.

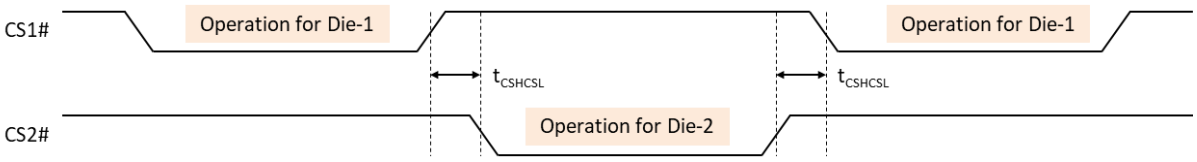


7.9.2 Multi-Die Memory Operation

CS# High time is defined only for consecutive instructions within the same die. See 8.7.4 CS# High Time and 8.7.5 AC Timing Parameters.



However, the time minimum interval time (t_{CSHCSL}) between CS1# (or CS2#) going High and CS2# (orCS1#) going Low is 0ns. Therefore, the device can be operated with no restriction for t_{CSD} or t_{CSDW} during die-interleaving operation.



8. Electrical Specifications

8.1 Absolute Maximum Ratings

Stresses greater that those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table 24: Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Voltage on Vcc Supply Relative to VSS : 3.3V Device	-0.5	3.8	V
Voltage on Any Pin relative to VSS : 3.3V Device	-0.5	3.8	V
Voltage on Vcc Supply Relative to VSS : 1.8V Device	-0.5	2.35	V
Voltage on Any Pin relative to VSS : 1.8V Device	-0.5	2.35	V
Storage Temperature	-55	150	°C
Operating Ambient Temperature	-40	85	°C
ESD HBM (Human Body Model)	≥ |2000 V|		V
ESD CDM (Charged Device Model)	≥ |500 V|		V
Solder Reflow Process	JEDEC J-STD-020 reflow profiles - Peak temperature ≤ 260°C - The time above 255°C ≤ 30 seconds - Reflow cycles ≤ 3 times		

8.2 Endurance, Retention and Magnetic Immunity

Table 25: Write Endurance, Retention and Magnetic Immunity

Parameter	Conditions	Min.	Max.	Units
Write Endurance	-25°C	10^{14}	-	cycles
Data Retention	85°C	10	-	years
Magnetic Field During Write or Read	-	-	24,000	A/m

8.3 Recommended Operating Conditions

Table 26: Recommended Operating Conditions

Parameter / Condition	Min.	Typ.	Max.	Units
Operating Temperature	-40	25	85	°C
Vcc Supply Voltage: 3.3V Device	2.7	3.3	3.6	V
Vcc Supply Voltage: 1.8V Device	1.71	1.8	1.98	V
Vss Supply Voltage	0.0	0.0	0.0	V

8.4 Pin Capacitance

Table 27: Pin Capacitance

Parameter	Conditions	Typ.	Max.	Units
Input Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V	-	8	pF
Input/Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; $V_{I/O}$ = 0V	-	18	pF

Note: Capacitance is sampled and not 100% tested

8.5 AC Test Condition

Table 28: AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to Vcc
Input rise and fall times	1ns/1V
Input and output measurement timing levels	Vcc/2
Output Load	CLoad = 30pF

8.6 DC Characteristics

Table 29: DC Characteristics: 3.3V Device

Parameter	Symbol	Test Conditions	2.7V-3.6V			Units
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 0 to Vcc (max)	-2	-	2	µA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to Vcc (max)	-2	-	2	µA
Read Current (1-1-1)	I_{CCR}	SDR=108MHz, DDR=54MHz CS1#=0 or CS2#=0, CLK=0/Vcc, I_{OUT}=0mA	-	9	12	mA
Read Current (2-2-2)	I_{CCR}		-	12	16	mA
Read Current (4-4-4)	I_{CCR}		-	15	20	mA
Write Current (1-1-1)	I_{CCW}	SDR=108MHz, DDR=54MHz CS1#=0 or CS2#=0, CLK=0/Vcc, I/O=0/Vcc	-	13	17	mA
Write Current (2-2-2)	I_{CCW}		-	18	24	mA
Write Current (4-4-4)	I_{CCW}		-	32	42	mA
Standby Current	I_{SB}	CLK=0, CS1# and CS2# =Vcc, I/O=0/Vcc	-	1.4	2.0	mA
Deep Power Down Current	I_{DPD}	CLK=0, CS1# and CS2# =Vcc, I/O=0/Vcc	-	340	800	µA
Input High Voltage	V_{IH}	-	0.7xVcc	-	Vcc+0.3	V
Input Low Voltage	V_{IL}	-	-0.3	-	0.2xVcc	V
Output High Voltage Level	V_{OH}	I_{OH} = -1mA	2.4	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2mA	-	-	0.4	V

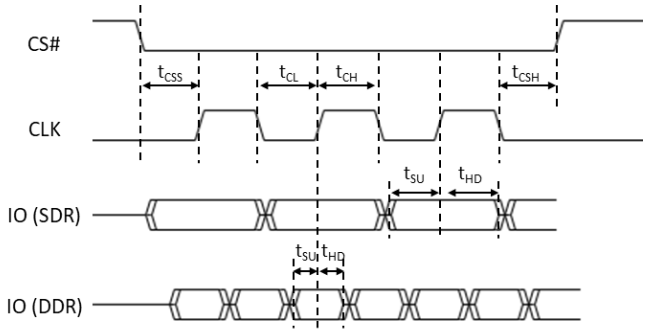
Table 30: DC Characteristics: 1.8V Device

Parameter	Symbol	Test Conditions	1.71V~1.98V			Units
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 0 to Vcc (max)	-2	-	2	µA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to Vcc (max)	-2	-	2	µA
Read Current (1-1-1)	I_{CCR}	SDR=108MHz, DDR=54MHz CS1#=0 or CS2#=0, CLK=0/Vcc, I_{OUT}=0mA	-	7	9	mA
Read Current (2-2-2)	I_{CCR}		-	8	11	mA
Read Current (4-4-4)	I_{CCR}		-	10	13	mA
Write Current (1-1-1)	I_{CCW}	SDR=108MHz, DDR=54MHz CS1#=0 or CS2#=0, CLK=0/Vcc, I/O=0/Vcc	-	10	13	mA
Write Current (2-2-2)	I_{CCW}		-	15	20	mA
Write Current (4-4-4)	I_{CCW}		-	26	34	mA
Standby Current	I_{SB}	CS1# and CS2# =Vcc, CLK=0, I/O=0/Vcc	-	1.2	1.8	mA
Deep Power Down Current	I_{DPD}	CS1# and CS2# =Vcc, CLK=0, I/O=0/Vcc	-	120	580	µA
Input High Voltage	V_{IH}	-	0.7xVcc	-	Vcc+0.3	V
Input Low Voltage	V_{IL}	-	-0.3	-	0.3xVcc	V
Output High Voltage Level	V_{OH}	I_{OH} = -1mA	1.4	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2mA	-	-	0.4	V

8.7 AC Timing Characteristics

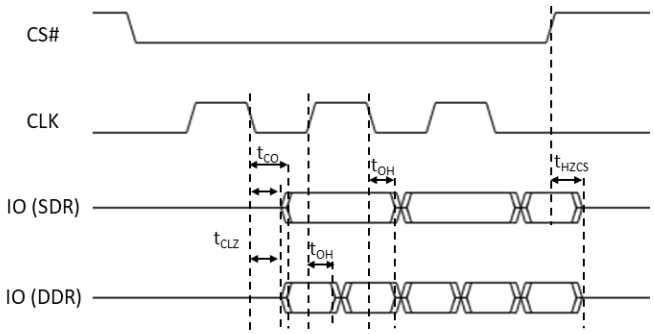
8.7.1 Synchronous Input Timing

Figure 29: Synchronous Input Timing (SDR/DDR)



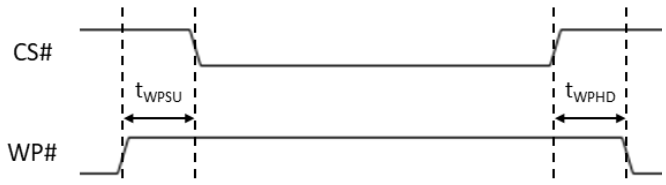
8.7.2 Synchronous Output Timing

Figure 30: Synchronous Data Output Timing (SDR/DDR)



8.7.3 WP# Timing

Figure 31: WP# Operation Timing



8.7.4 CS# High Time

CS# High time (the period during which CS# signal remains High) is divided into five timing based on operations.

1) CS# High time after any Read instructions, Write Enable/Disable, Enable Quad/Dual/Extended SPI, No Operation and Software Reset Enable.
2) CS# High time after Write Memory instructions.
3) CS# High time after Write Register instructions or Augmented Area instruction.
4) CS# High time to deep power down exit.
5) CS# High time after JEDEC reset and software reset operation.

Notes:
1. CS# High time is defined only for consecutive instructions within the same die.

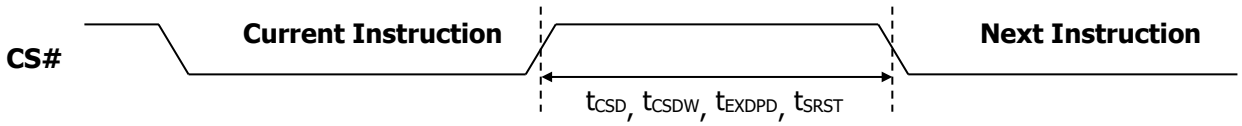


Table 31: CS# High time after instructions

Parameter	Symbol	Min	Max.	Unit
CS# High time after any Read instructions, Write Enable/Disable, Enable Quad/Dual/Extended SPI, No Operation and Software Reset Enable	t_{CSD}	20	-	ns
CS# High time after Write Memory instructions	t_{CSDW}	Refer to Table 33		-
CS# High time after Write Register instructions or Augmented Area instruction	t_{CSDW}	Refer to Table 34		-
CS# High time after deep power down exit command	t_{EXDPD}	25	-	us
CS# High time after JEDEC reset and software reset (3.3V Device)	t_{SRST}	0.3	-	ms
CS# High time after JEDEC reset and software reset (1.8V Device)	t_{SRST}	2.0	-	ms

Notes:
1. Read Status Register (05h) instruction is applicable during any CS# High period.

8.7.5 AC Timing Parameters

Table 32: AC Timing Parameter

Parameter	Symbol	Min.	Max.	Units
Clock Frequency – SDR	f_{CLK}	1	108	MHz
Clock Frequency – DDR	f_{CLK}	1	54	MHz
Clock Low Time	t_{CL}	0.45 * 1/ fCLK	-	ns
Clock High Time	t_{CH}	0.45 * 1/ fCLK	-	ns
CS# Setup Time	t_{CSS}	5	-	ns
CS# Hold Time	t_{CSH}	4	-	ns
CS# High Time after Any Instruction (except Write)	t_{CSD}	20	-	ns
CS# High Time after Write Instruction	t_{CSDWX}	Refer to Table 33, 34		
Data Setup Time	t_{SU}	2	-	ns
Data Hold Time	t_{HD}	2	-	ns
CLK Low to Output Valid	t_{CO}	-	7.0	ns
CLK to Output Hold Time	t_{OH}	2.0	-	ns
CLK Low to Output Low-Z (Read)	t_{CLZ}	2.0	-	ns
CS# High to Output High-Z	t_{HZCS}	-	6.0	ns
WP# Setup Time	t_{WPSU}	20	-	ns
WP# Hold Time	t_{WPHD}	20	-	ns
CS# High to Power-down mode	t_{EDPD}	-	1	us
CS# High to Power-down mode exit	t_{EXDPD}	-	25	us
CS# Low time to exit Power-down mode	t_{CSDPD}	50	-	ns
The time minimum interval time (t_{CSHCSL}) between CS1# (or CS2#) going High and CS2# (orCS1#) going Low	t_{CSHCSL}	0	-	ns
Software Reset Time (3.3V Device)	t_{SRST}	-	0.3	ms
Software Reset Time (1.8V Device)	t_{SRST}	-	2.0	ms

Table 33: CS# High Time after Write Memory Instruction

Current Instruction : Write Memory	Next Instruction : Read or Write Memory	Symbol	Operating Frequency, SDR						Units
			108	100	83	66	54	40	
1s-1s-1s, 1s-Xs-2s	1s-1s-Xs	t_{CSDW1}	20	20	20	20	20	20	ns
1s-1s-1s, 1s-Xs-2s	1s-2s-2s	t_{CSDW1}	130	120	70	20	20	20	ns
1s-1s-1s, 1s-Xs-2s	1s-4s-4s	t_{CSDW1}	190	180	150	100	50	20	ns
1s-Xs-4s	1s-1s-Xs	t_{CSDW1}	130	100	20	20	20	20	ns
1s-Xs-4s	1s-2s-2s	t_{CSDW1}	260	230	150	20	20	20	ns
1s-Xs-4s	1s-4s-4s	t_{CSDW1}	300	280	210	100	50	20	ns
2s-2s-2s	2s-2s-2s	t_{CSDW1}	170	160	120	70	20	20	ns
4s-4s-4s	4s-4s-4s	t_{CSDW1}	350	330	280	190	170	100	ns

Current Instruction : Write Memory	Next Instruction : Read or Write Memory	Symbol	Operating Frequency, DDR						Units
					54	40	33	27	
1s-1d-1d, 1s-Xd-2d	1s-1d-Xd	t_{CSDW2}			20	20	20	20	ns
1s-1d-1d, 1s-Xd-2d	1s-2d-2d	t_{CSDW2}			50	20	20	20	ns
1d-1d-1d, 1s-Xd-2d	1s-4d-4d	t_{CSDW2}			100	30	20	20	ns
1s-Xd-4d	1s-1d-Xd	t_{CSDW2}			50	20	20	20	ns
1s-Xd-4d	1s-2d-2d	t_{CSDW2}			160	20	20	20	ns
1s-Xd-4d	1s-4d-4d	t_{CSDW2}			210	70	20	20	ns
2s-2d-2d	2s-2d-2d	t_{CSDW2}			120	50	20	20	ns
4s-4d-4d	4s-4d-4d	t_{CSDW2}			320	210	150	100	ns

Notes:
1. The CS# High time after Write Memory instructions is strongly dependent on SPI mode and frequency.

Table 34: CS# High Time after Register/Augmented Area Write Instruction

Current Instruction	Next Instruction	Symbol	Min.	Units
Write Memory Instructions	Read Register except for Status Register Write Register Read or Write Augmented Area	t_{CSDW3}	500	ns
Write Register Instructions Write Augmented Area Instruction	Any Instructions except for Status Register	t_{CSDW4}	1000	ns

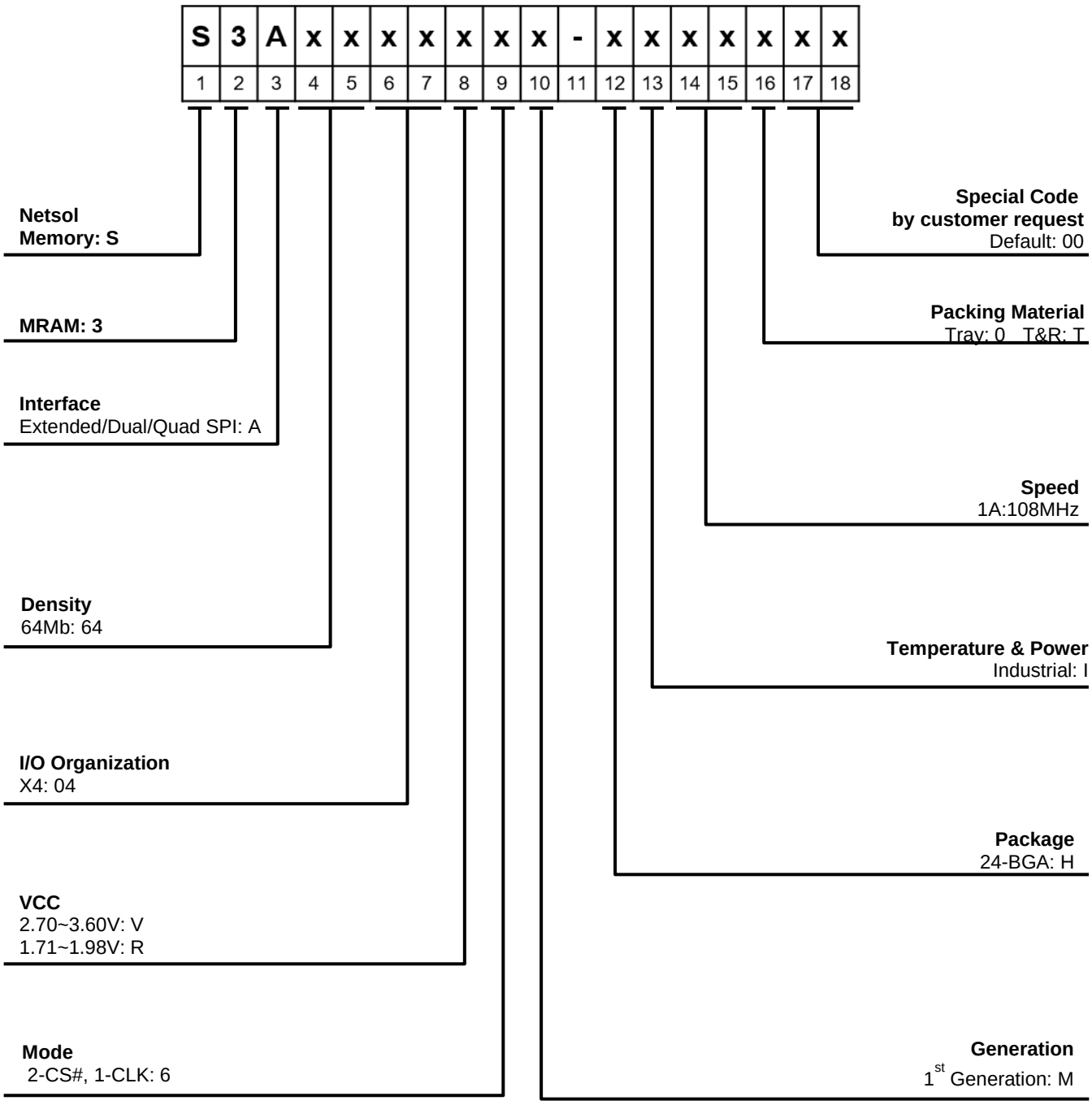
9. Thermal Resistance

Table 35: Thermal Resistance

Parameter	Description	24 BGA	Unit
θ_{JA}	Thermal resistance (junction to ambient)	69.2	°C/W
θ_{JC}	Thermal resistance (junction to case)	30.4	

Notes:
1: These parameters are guaranteed by characterization; not tested in production.

10. Part Numbering System



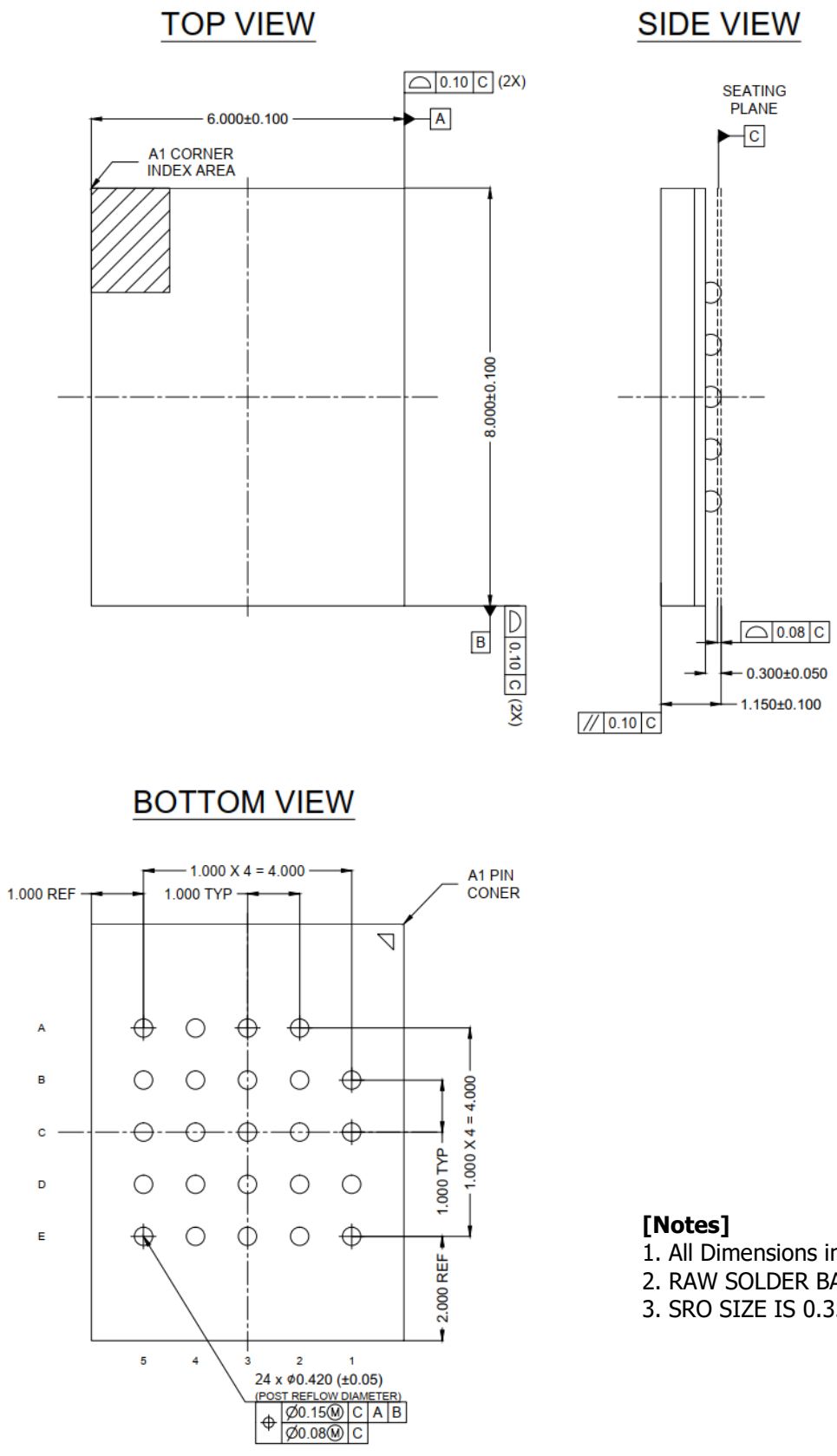
11. Ordering Part Numbers

Table 36: Ordering Part Number

Temperature Grade	Operating Temperature	Package	Voltage	Shipping Container	Ordering Part Number
Industrial	-40°C to 85°C	24 FBGA	3.3V	Tray	S3A6404V6M-HI1A000
				Tape and Reel	S3A6404V6M-HI1AT00
			1.8V	Tray	S3A6404R6M-HI1A000
				Tape and Reel	S3A6404R6M-HI1AT00

12. Package Dimension

24-Ball BGA (6mm x 8mm)



[Notes]
1. All Dimensions in Millimeters
2. RAW SOLDER BALL SIZE IS 0.40mm
3. SRO SIZE IS 0.35mm

Revision History

Revision	Date	Description
0.1	Mar, 2025	Initial Release

* Products and specifications discussed herein are subject to change by Netsol without notice.